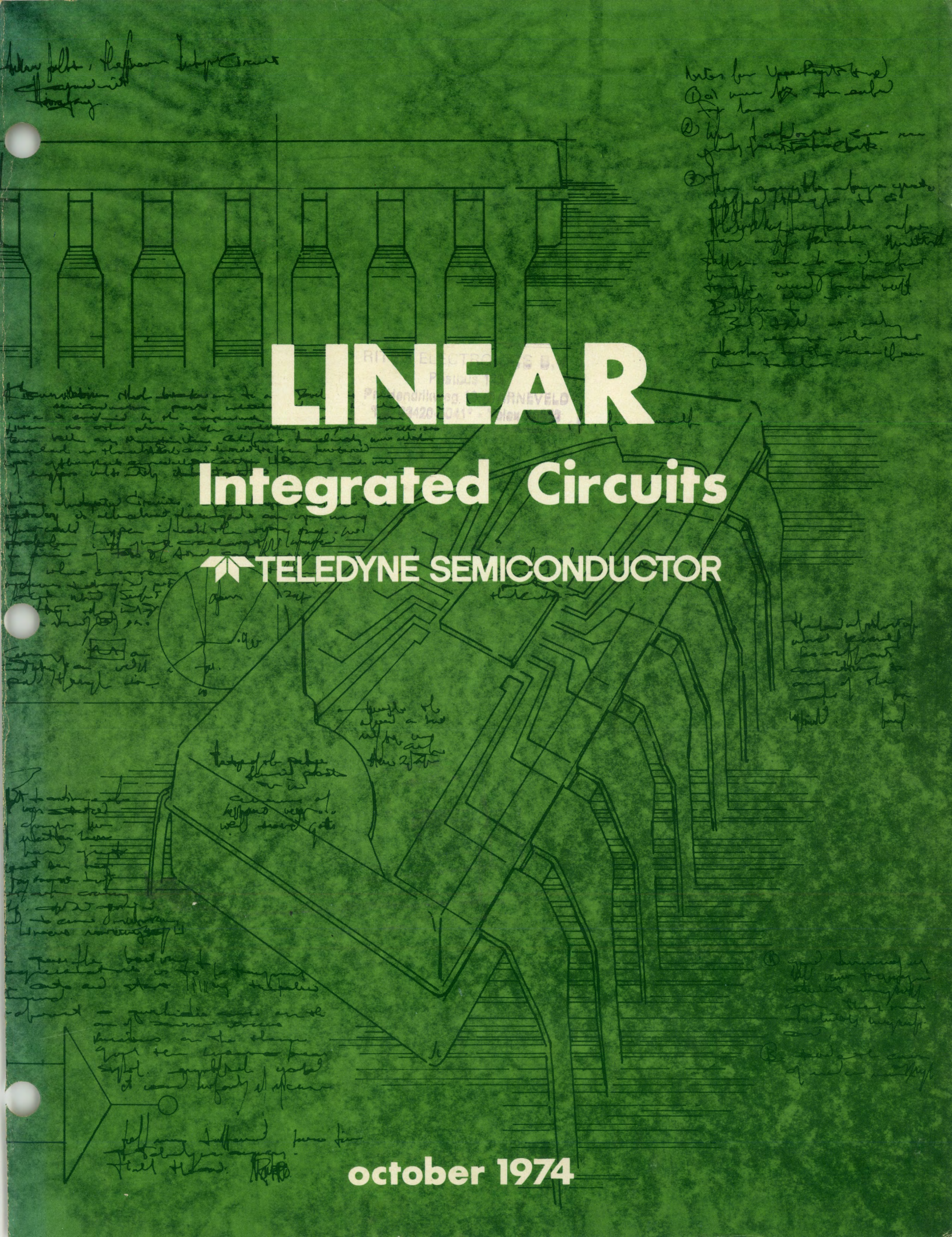


LINEAR

Integrated Circuits

TELEDYNE SEMICONDUCTOR

october 1974

Linears from TELEDYNE SEMICONDUCTOR

Contents

Section I

Manufacturers' Cross Reference and Selection Guides

Linear Cross Reference Guide

This listing attempts to provide a handy and reliable guide to pin-for-pin equivalents for standard Teledyne linears. Additional product and package types may also be available from other manufacturers or on special order. While every effort has been made to insure accuracy, we cannot accept responsibility for the consequences of any errors or omissions in this guide.

National	Motorola	Fairchild
LM101AD	–	LM101AD
AF	–	AF
AH	MLM101AG	AH
LM104F	–	–
H	MLM104G	LM104H
LM105F	–	–
H	MLM105G	LM105H
LM107D	–	–
F	–	–
H	MLM107G	LM107H
LM111D	–	–
F	–	–
H	–	LM111H
LM124D	–	–
F	–	–
LM139F	–	–
D	–	–
LM201AD	–	LM201AD
AF	–	–
AH	MLM201AD	AH
LM204H	MLM204G	–
LM205F	–	–
H	MLM205G	–
LM207D	–	–
F	–	–
H	MLM207G	LM207H
LM211D	MLM211L	–
F	F	–
H	–	LM211H
LM224D	–	–
N	–	–
LM239D	–	–
LM301AD	–	LM301AD
AH	MLM301AG	AH
AN	AP1	AN
LM304H	MLM304G	LM304H
LM305AH	–	LM305AH
H	MLM305G	H

TELEDYNE	Page
LM101AD	2
AF	
AH	
LM104F	68
H	
LM105F	74
H	
LM107D	8
F	
H	
LM111D	106
F	
H	
LM124D	11
F	
LM139F	112
D	
LM201AD	2
AF	
AH	
LM204H	68
LM205F	74
H	
LM207D	8
F	
H	
LM211D	106
F	
H	
LM224D	11
N	
LM239D	112
LM301AD	2
AH	
AN	
LM304H	68
LM305AH	74
H	

National	Motorola	Fairchild
LM307D	–	–
H	MLM307G	LM307H
N-8	–	N
LM308AD	–	LM308AD
AH	–	AH
D	–	D
H	–	H
N	–	–
LM311D	MLM311L	–
H	–	LM311H
N-8	–	–
LM324D	–	–
N	–	–
LM339D	–	–
N-14	–	–
LM376N	–	LM376N
LM709AH	–	709AHM
–	–	ADM
LM709AF	–	AFM
H	MC1709G	HM
–	–	FM
–	MC1709L	DM
LM709CH	CG	HC
CN-14	CP2	–
–	CL	709DC
LM710H	MC1710G	710HM
–	–	FM
–	MC1710L	DM
LM710CH	CG	HC
–	CL	DC
LM711H	MC1711G	711HM
–	–	FM
–	MC1711BL	DM
LM711CH	CG	HC
CN	–	–
–	MC1711CL	711DC
LM723H	MC1723G	723HM
–	MC723L	DM
LM723CH	MC1723CG	HC
CN-14	–	–
–	MC723CL	723DC
LM741H	MC1741G	741HM
F	F	FM
D	L	DM
CH	CG	HC
CN	CP1	TC
CN-14	CP2	–

TELEDYNE	Page
LM307D	8
H	
N-8	
LM308AD	16
AH	
D	
H	
N	
LM311D	106
H	
N-8	
LM324D	11
N	
LM339D	112
N-14	
LM376N	81
709AE	20
AL	
AH	
BE	
BH	
BL	
CE	
CJ	
CL	
710BE	115
BH	
BL	
CE	
CL	
711BE	117
BH	
BL	
CE	
CJ	
CL	
723BE	84
BL	
CE	
CJ	
CL	
741BE	27
BH	
BL	
CE	
CP	
CJ	

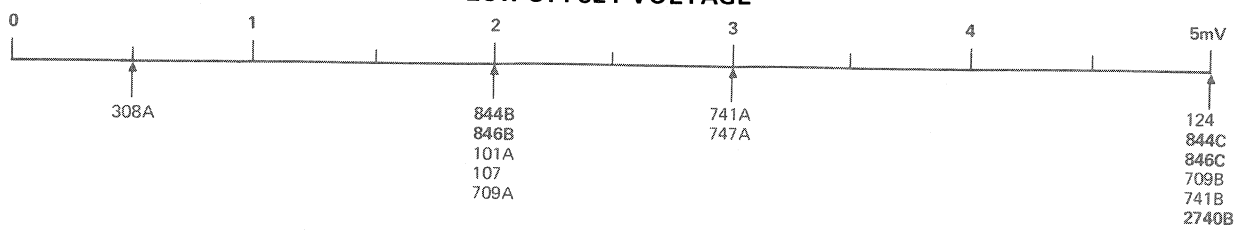
National	Motorola	Fairchild	TELEDYNE	Page
LM747H	–	747HM	747BE	34
H	MC1747F	FM	BH	
D	L	DM	BL	
CH	–	HC	CE	
CN-14	–	–	CJ	
CD	MC1747CL	747DC	CL	
LM748H	MC1748G	748HM	748BE	40
H	–	FM	BH	
–	–	DM	BL	
LM748CH	MC1748CG	HC	CE	
–	–	DC	CL	
LM748CN	–	TC	CP	
LM1458H	MC1458G	MC1458G	1458E	60
N	P1	P1	P	
–	CG	CG	CE	
–	CP1	CP1	CP	
LM1558H	MC1558G	MC1558G	1558E	60
LH0042H	–	740HM	2740BE	62
CH	–	HC	CE	
–	–	–	DE	
LM2901N	–	–	LM2901N	120
–	MC3302P	–	J	
LM75450N	MC75450P	SN75450AN	75450J	125

National	Motorola	Fairchild	TELEDYNE	Page
51N	51P	51AP	51P	125
52N	52P	52P	52P	
53N	53P	53P	53P	
54N	54P	54P	54P	
–	–	SN75460AN	75460J	125
–	–	61AP	61P	
–	–	62AP	62P	
–	–	63AP	63P	
–	–	64AP	64P	
–	–	78M05HM	78M05BE	99
–	–	06HM	06BE	
–	–	08HM	08BE	
–	–	12HM	12BE	
–	–	15HM	15BE	
–	–	20HM	20BE	
–	–	24HM	24BE	
–	–	05HC	05CE	
–	–	06HC	06CE	
–	–	08HC	08CE	
–	–	12HC	12CE	
–	–	15HC	15CE	
–	–	20HC	20CE	
–	–	24HC	24CE	
	Exar XR2556 CP		D555CJ	136
	Signetics NE556A		556CJ	142

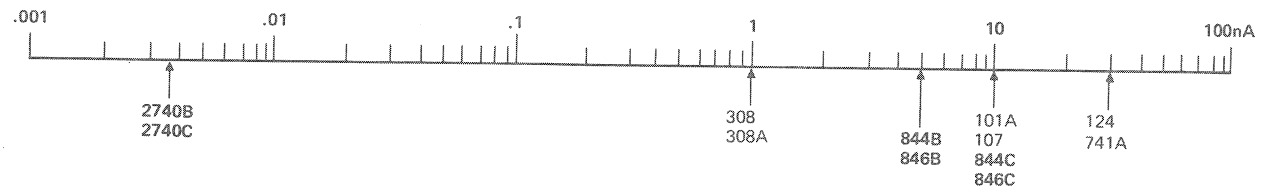
Selection Guide

Operational Amplifiers

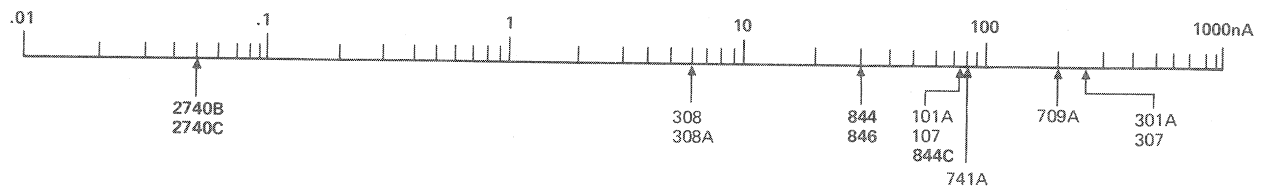
LOW OFFSET VOLTAGE



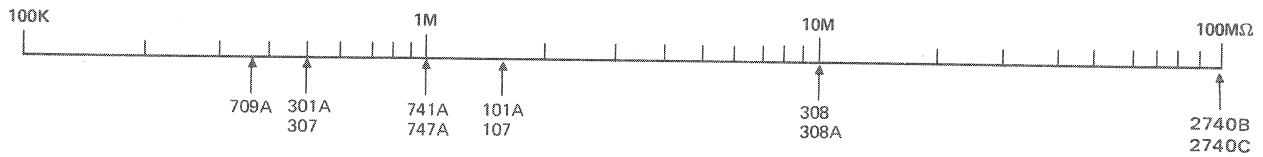
LOW OFFSET CURRENT



LOW BIAS CURRENT

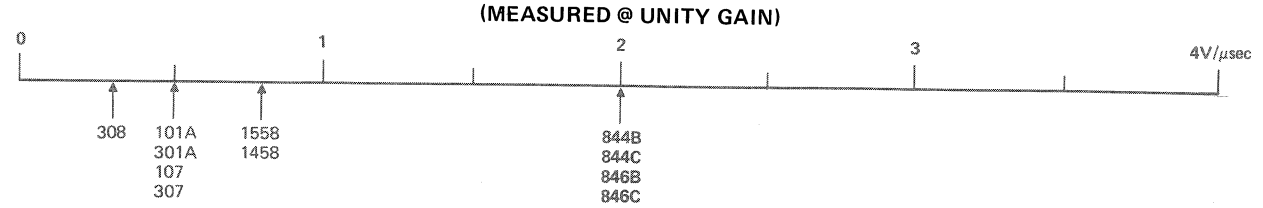


HIGH INPUT RESISTANCE



HIGH SLEW RATE

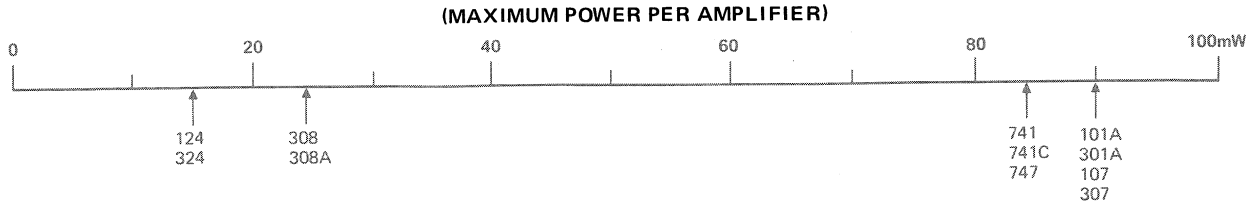
(MEASURED @ UNITY GAIN)



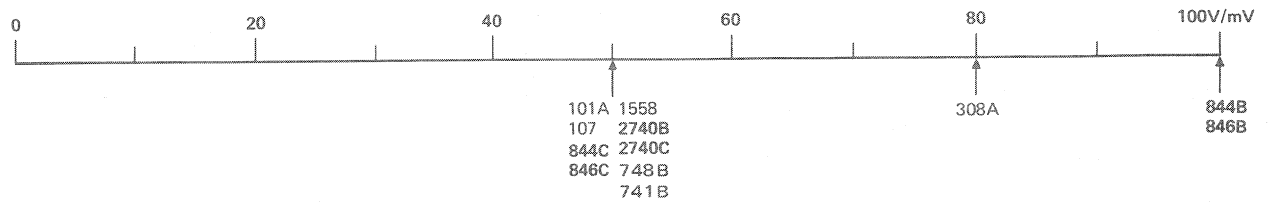
Bold face type indicates Teledyne Semiconductor proprietary products.

Operational Amplifiers (Cont'd.)

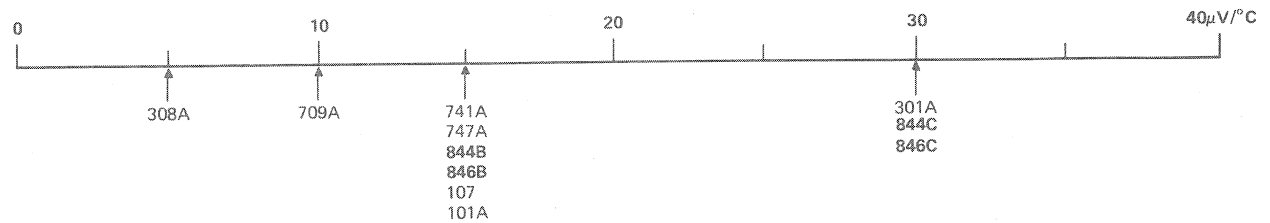
LOW POWER
(MAXIMUM POWER PER AMPLIFIER)



VOLTAGE GAIN (MINIMUM GUARANTEED)

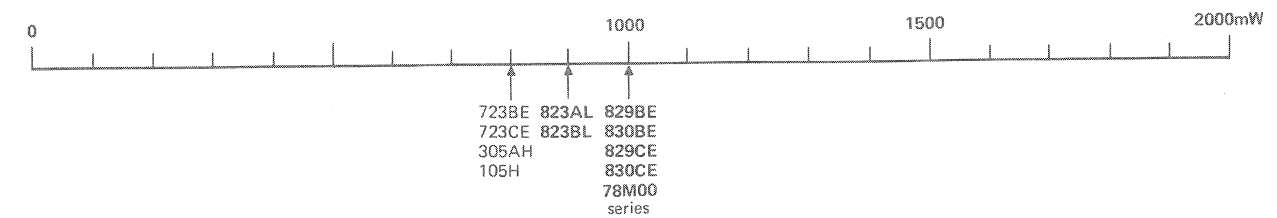


LOW OFFSET VOLTAGE DRIFT

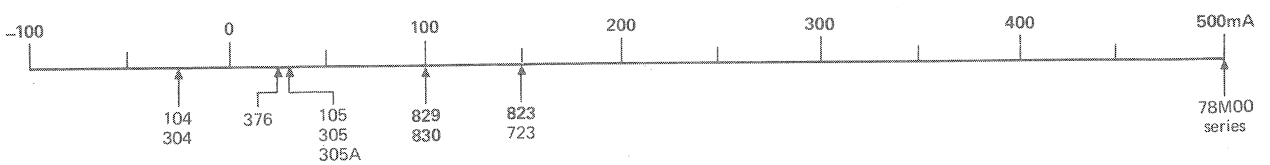


Voltage Regulators

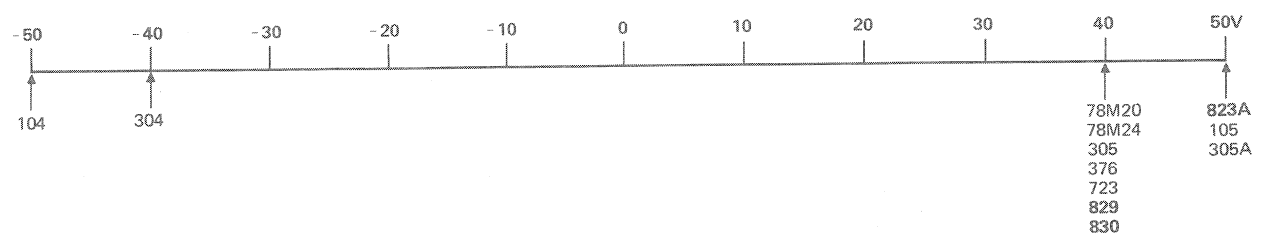
POWER DISSIPATION



LOAD CURRENT



MAXIMUM INPUT VOLTAGE



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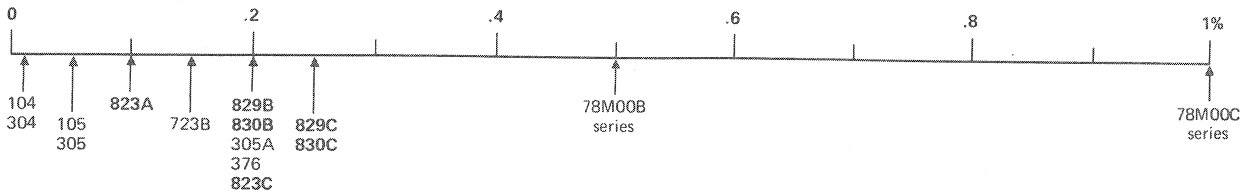
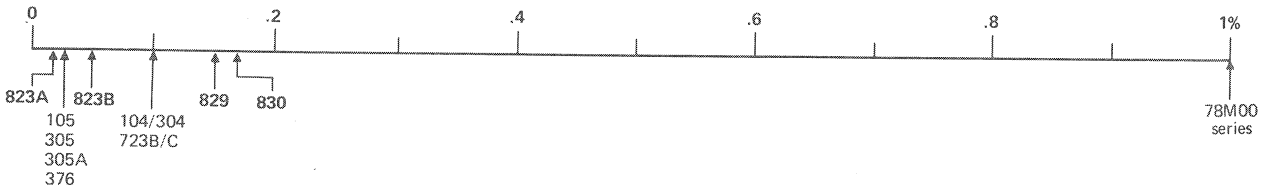
Voltage Regulators (Cont'd.)

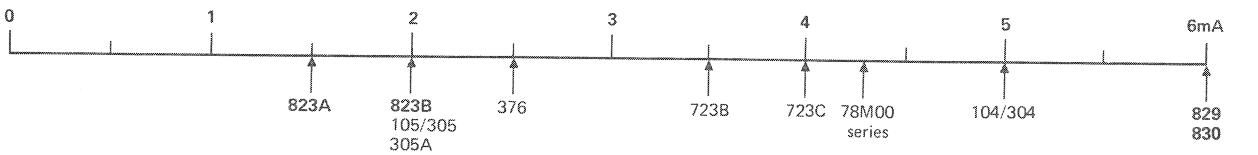
LOAD REGULATION



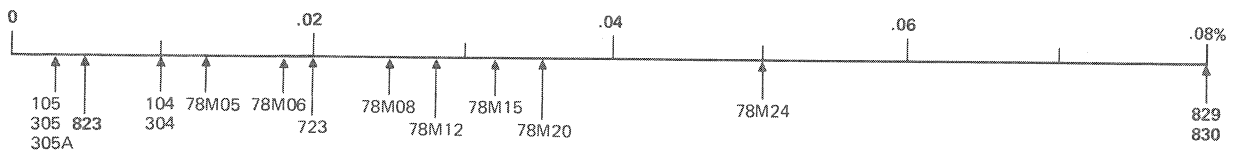
LINE REGULATION



STANDBY CURRENT

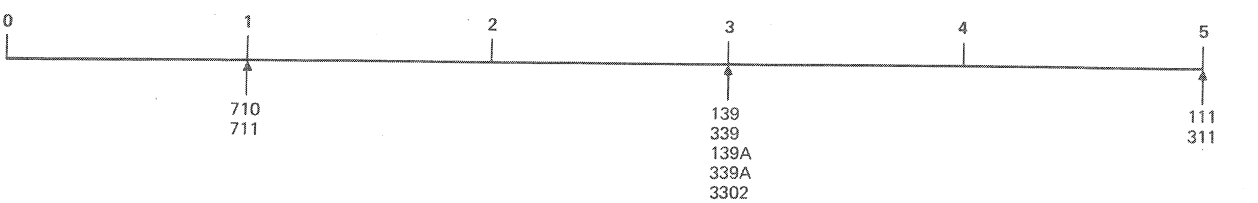


RIPPLE REJECTION

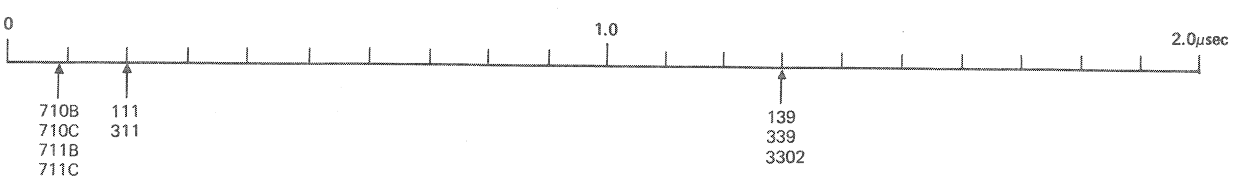


Comparators

MAXIMUM OUTPUT FANOUT



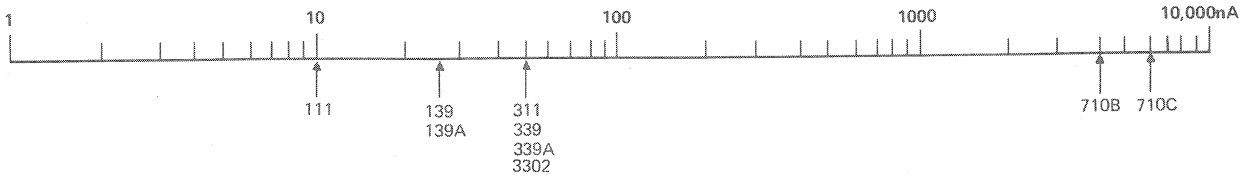
HIGH SPEED



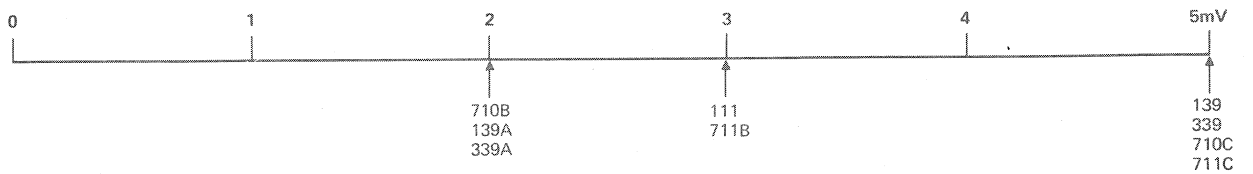
Bold face type indicates Teledyne Semiconductor proprietary products.

Comparators (Cont'd.)

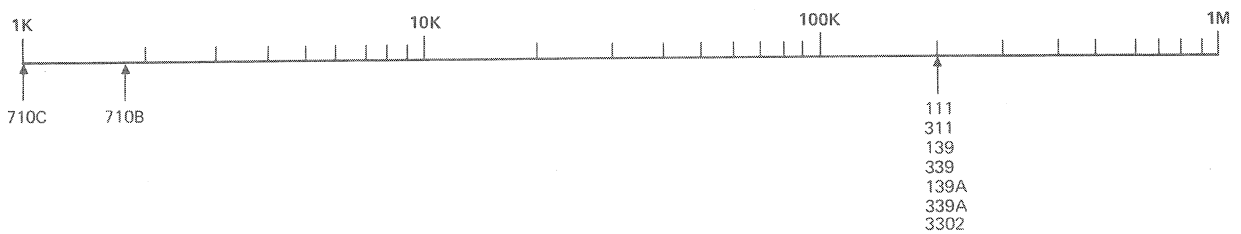
LOW INPUT OFFSET CURRENT



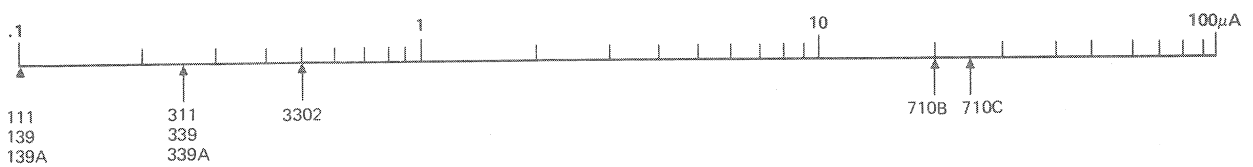
LOW INPUT OFFSET VOLTAGE



HIGH GAIN



LOW BIAS CURRENT



Bold face type indicates Teledyne Semiconductor proprietary products.

Quality and Reliability

Teledyne Semiconductor's standard quality control operations and process flows have been designed to assure compliance with MIL-STD-883. A complete line of 883-processed linears as standard products. In addition, any Teledyne linear circuits can be tested to any class of MIL-STD-883. Our internal quality assurance manual is available for review upon request.

PROCESS FLOW

Table 1 shows the standard flow for Teledyne integrated circuits processed in conformance with MIL-STD-883 B. After wafer processing, special visual inspections are performed to MIL-STD-883, method 2010.1, condition B or A at both chip and preseal inspections to assure a packaged chip of high reliability. Class A products are tested functionally and then receive a DC parameter test. Significant parameters are recorded. A 240-hour burn-in at 125°C is then performed, after which all testing is repeated and delta shifts calculated. Parametric data for each device, is provided for the customer. This is followed by 100 percent high and low temperature testing under functional DC operating conditions. Next, 100 percent AC testing is accomplished, followed by Group A sampling of all test conditions. Class A products are branded, visually inspected, and retested to DC parameters prior to packaging and shipment.

Class B and Class C devices are processed in a similar manner, Class B devices undergo burn-in for 168 hours with GO NO-GO parameter readings made before and after burn-in. Temperature tests are done on a sample basis, and visual inspections are performed (although these are less critical than for Class A devices). Class C device processing is similar to Class B, but without burn-in, temperature, and AC tests.

STANDARD PROCESS FLOW SUMMARY

MANUFACTURING OPERATION	MANUFACTURING INSPECTION
Manufacturing Stores	Purchased Item Verification
Mask Making	Mask Inspection
Materials Preparation	Wafer Preparation and Epitaxial Growing

STANDARD PROCESS FLOW SUMMARY (Cont'd.)

MANUFACTURING OPERATION	MANUFACTURING INSPECTION
Photoengraving & Diffusion	Electrical Probe Check and 100% Visual Inspection
Final Wafer Lot Acceptance	100% Visual Inspection
Electrical Test of Wafer	100% Electrical Test
Scribing and Dicing	100% Visual Inspection
Visual Die Sort MIL-STD-883 Method 2010.1, Condition B	100% Die Sort Inspection
Die Attach	100% Visual Inspection
Lead Bond	100% Visual Inspection
Pre-Seal Inspection **At 100X Magnification** MIL-STD-883 Method 2010.1, Condition B	100% Visual Inspection at High-Power Magnification
At 30X Magnification MIL-STD-883 Method 2010.1, Condition B	100% Visual Inspection at Low-Power Magnification
Final Seal	Visual & Hermeticity
High-Temperature Bake 150°C – 24 hours minimum (MIL-STD-883, Method 1010, Condition C)	100% Processing
Temperature Cycling −65°C to +150°C, 10 Cycles (MIL-STD-883, Method 1010, Condition C)	100% Processing
Centrifuge 30 KG Min. Y_1 Axis (MIL-STD-883, Method 2001, Condition E)	100% Processing
Lead Form	100% Visual Inspection
Carrier Load	100% Visual Inspection
Hermeticity MIL-STD-883, Method 1014	
External Visual	100% Inspection
Electrical Test & Sort	100% Inspection

QUALITY INSPECTION GUARANTEE

INSPECTION		LTPD/MAX. ACC. NO.	COMMENTS
External		15/2	MIL-STD-833, Method 2009
Hermeticity		10/2	
Fine Leak			MIL-STD-883, Method 1014, Condition A
Gross Leak			MIL-STD-883, Method 1014, Condition E (Proposed), Weight Method
Electrical			
Static Parameters	+25°C	10/2	Per Applicable Electrical Test Specification
	+125°C	15/2	
	−55°C	15/2	
Dynamic Parameters	+25°C	10/2	
	+125°C	15/2	
	−55°C	15/2	
Package and Ship		(Quality Assurance Monitor Per QR5560)	

STANDARD SCREENING PROCEDURES

GROUP A ELECTRICAL TESTS — MIL-STD-883

SUBGROUPS	CLASS A LTPD	CLASS B LTPD	CLASS C LTPD
Subgroup 1 Static tests at 25°C	5	5	5
Subgroup 2 Static tests at maximum rated operating temperature	5	7	10
Subgroup 3 Static tests at minimum rated operating temperature	5	7	10
Subgroup 4 Dynamic tests at 25°C	5	5	5
Subgroup 5 Dynamic tests at maximum rated operating temperature	5	7	10
Subgroup 6 Dynamic tests at minimum rated operating temperature	5	7	10
Subgroup 7 Functional tests at 25°C	3	5	5
Subgroup 8 Functional tests at maximum and minimum rated operating temperatures	5	10	15
Subgroup 9 Switching tests at 25°C	5	7	10
Subgroup 10 Switching tests at maximum rated operating temperature	5	10	15
Subgroup 11 Switching tests at minimum rated operating temperature	5	10	15

NOTE:

The specific parameters to be included for tests in each subgroup shall be as specified in the applicable reliability specification. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing shall be performed for that subgroup or test to satisfy group A requirements.

STANDARD SCREENING PROCEDURES (Cont'd.)

GROUP B TESTS, MIL-STD-883, METHOD 5005

	TEST	METHOD	CONDITION	CLASS A LTPD	CLASS B LTPD	CLASS C LTPD
Subgroup 1	Physical	2008	Test condition A	10	15	20
Subgroup 2	Marking permanency	2008	Test condition B	4 devices (no failures)	4 devices (no failures)	4 devices (no failures)
	Visual and mechanical	2008	Test condition B with criteria from design and construction requirements of applicable reliability specification	1 device (no failures)	1 device (no failures)	1 device (no failures)
	Bond strength	2011				
	Thermocompression		Test condition C or D	5	15	20
	Ultrasonic or wedge		Test condition C or D			
Subgroup 3	Solderability	2003	Soldering temperature of 260 ± 10°C	10	15	15
Subgroup 4	Lead fatigue	2004	Test condition B_2	10	15	15
	Hermeticity: Fine, Gross	1014	Per applicable reliability specification			

GROUP C TESTS, MIL-STD-883, METHOD 5005

	TEST	METHOD	CONDITION	CLASS A LTPD	CLASS B LTPD	CLASS C LTPD
Subgroup 1	Thermal shock	1011	Test condition B as a minimum	10	15	15
	Temperature cycling	1010	Test condition C			
	Moisture resistance	1004	Omit initial conditioning			
	Hermeticity: Fine, Gross	1014	As applicable			
	End point electrical parameters		As specified in the applicable reliability specification			
Subgroup 2	Mechanical shock	2002	Test condition B	10	15	15
	Vibration, variable frequency	2007	Test condition A			
	Constant acceleration	2001	Test condition E			
	Hermeticity: Fine, Gross	1014	Per applicable reliability specification			
	End point electrical parameters		As specified in the applicable reliability specification			

GROUP C TESTS, MIL-STD-883, METHOD 5005 (Cont'd.)

TEST		METHOD	CONDITION	CLASS A LTPD	CLASS B LTPD	CLASS C LTPD
Subgroup 3	Salt atmosphere	1009	Test condition A. Omit initial conditioning	10	15	15
Subgroup 4	High temperature storage End point electrical parameters	1008	150^{+50}_{-25} °C storage, 1000 hrs. As specified in the applicable reliability specification	7	7	7
Subgroup 5	Operating life test End point electrical parameters	1005	Test condition to be specified in the applicable reliability specification (1000 hrs.) As specified in the applicable reliability specification	5	5	5
Subgroup 6	Steady state reverse bias End point electrical parameters	1005	Test condition A, 72 hrs. at 150°C As specified in the applicable reliability specification	7		

OPTIONAL SCREENING PROCEDURES

To minimize reliability for critical applications, the optional procedures shown below provide for all three levels of screening per MIL-STD-883, Method 5004. This series is available at extra cost and is applied after normal Group A acceptance tests. Parametric test data for individual variables is supplied with each Class A device.

OPTIONAL SCREENING PROCEDURES (MIL-STD-883, METHOD 5004.1)

SCREEN	CLASS A		CLASS B		CLASS C	
	METHOD	REQUIREMENT	METHOD	REQUIREMENT	METHOD	REQUIREMENT
Internal visual (Precap)	2010.1, test condition A	100%	2010.1, test condition B	100%	2010.1, test condition B	100%
Stabilization bake	1008, 24 hrs. test condition C, 150°C	100%	1008, 24 hrs. test condition C, 150°C	100%	1008, 24 hrs. test condition C, 150°C	100%
Thermal shock	1011, test condition A, 0°C-100°C 15 cycles	100%	Not required		Not required	
Temperature cycling	1010, test condition C, −55°C to +100°C, 10 cycles	100%	1010, test condition C, −55°C to +100°C, 10 cycles	100%	1010, test condition C, −55°C to +100°C, 10 cycles	100%
Mechanical shock	2002, test condition B five shock pulses in Y_1 plane only	100%	Not required		Not required	
Constant acceleration	2001, test condition E Y_2 plane, then Y_1 plane, 30,000 G's	100%	2001, test condition E Y_1 plane, 30,000 G's	100%	2001, test condition E Y_1 plane, 30,000 G's	100%

OPTIONAL SCREENING PROCEDURES (Cont'd.)

SCREEN	CLASS A		CLASS B		CLASS C	
	METHOD	REQUIREMENT	METHOD	REQUIREMENT	METHOD	REQUIREMENT
Seal Fine, Gross	1014, Condition A Condition C	100%	1014, Condition A Condition C	100%	1014, Condition A Condition C	100%
Critical electrical parameters	Read and record	100%	Go No-Go		Not required	
Burn-in test	1015, 240 hrs. @ $T_A = 125°C$ per applicable reliability specification	100%	1015, 168 hrs. @ $T_A = 125°C$ per applicable reliability specification	100%	Not required	
Critical electrical parameters	Read and record per applicable reliability specification	100%	Not required		Not required	
Reverse bias burn-in	1015, test condition A or C, 72 hrs. @ 150°C	100%	Not required		Not required	
Final electrical tests	Per applicable reliability specifications		Per applicable reliability specifications		Per applicable reliability specifications	
Static tests 25°C		100%		100%		100%
Maximum and minimum rated operating temp.		100%		100%		
Dynamic tests and switching tests 25°C		100%		100%		
Functional test 25°C (subgroup 7, table 1, 5005)		100%		100%		100%
Radiographic	2012	100%	Not required		Not required	
Qualification or quality conformance inspection Groups B and C optional, at extra cost	5005 Class A	Per 38510	5005 Class B	Per 38510	5005 Class C	Per 38510
External visual	2009	100%	2009	100%	2009	100%

MIL-M-38510 QUALIFICATION

Teledyne Semiconductor is pursuing a program to qualify a number of its standard linear devices in accordance with MIL-M-38510 "JAN" requirements. Until complete qualification is received, these products are available as "MIL-M-38510 processed" devices, built in compliance with MIL-M-38510 general requirements and MIL-STD-883 test methods and procedures. Testing of "MIL-M-38510 processed" devices is done either to slash-sheet electrical limits or to Teledyne data sheet specifications. For additional information on Teledyne MIL-M-38510 qualification and on devices available as "MIL-M-38510 processed", contact your Teledyne Semiconductor sales office.

Section II
Operational Amplifiers

101A Series

101A•201A•301A

Operational Amplifiers

Features

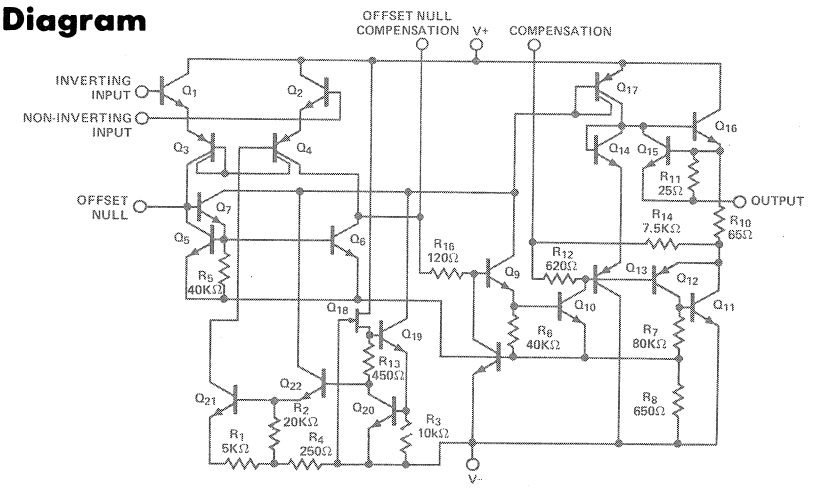
- LOW OFFSET VOLTAGE – 3mV
- LOW INPUT BIAS CURRENT – 100nA MAX
- LOW OFFSET CURRENT – 20nA MAX
- OFFSETS GUARANTEED OVER ENTIRE COMMON MODE RANGE
- CONTINUOUS SHORT CIRCUIT PROTECTION
- GUARANTEED DRIFT CHARACTERISTICS

Description

The Teledyne 101A, 201A and 301A are general purpose, high performance operational amplifiers fabricated monolithically on a silicon chip by the planar epitaxial process.

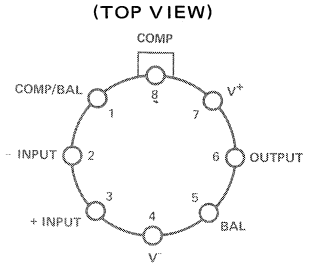
These high performance integrated circuits are intended for applications requiring low input offset voltage or low input offset current. The accuracy of long interval integrators, timers and sample and hold circuits is improved due to the low drift and low bias currents. This amplifier offers many features which make its application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, freedom from oscillations and compensation with a single 30pF capacitor. The 101A operational amplifier will operate over the full military temperature range from −55°C to +125°C. The commercial version, the 301A, operates over a temperature range from 0°C to +70°C. The 201A is the same as the 101A except its performance is guaranteed from −25°C to +85°C.

Equivalent Circuit Diagram



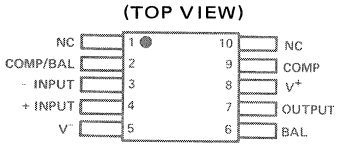
Connection Diagrams

E PACKAGE
8 LEAD METAL CAN
(TOP VIEW)



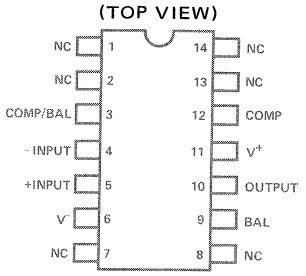
Order Part Numbers:
LM101AH, LM201AH,
LM301AH

H PACKAGE
10 LEAD FLATPACK
(TOP VIEW)



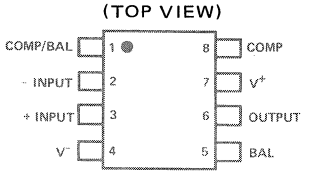
Order Part Number:
LM101AF

L PACKAGE
14 LEAD CERDIP
(TOP VIEW)



Order Part Numbers:
LM101AD, LM201AD,
LM301AD

P PACKAGE
8 LEAD MINIDIP
(TOP VIEW)



Order Part Number:
LM301AN

Absolute Maximum Ratings

Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Output Short Circuit Duration (Note 2)	Indefinite
Supply Voltage	
101A	±22V
201A	±22V
301A	±18V
Power Dissipation (Note 3)	500mW
Operating Temperature Range	
101A	−55°C to +125°C
201A	−25°C to +85°C
301A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60s)	300°C

Electrical Characteristics

PARAMETER	CONDITIONS	101A			301A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 10K\Omega$		0.7	2.0		1.5	5.0	mV
Input Offset Current	$T_A = 25°C$		1.5	10		3	20	nA
Input Bias Current	$T_A = 25°C$		30	75		70	250	nA
Input Resistance	$T_A = 25°C$	1.5	4		0.5	2		MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 20V$		1.8	3.0		1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2K\Omega$	50	160		25	160		V/mV
Input Offset Voltage	$R_S \leq 10K\Omega$			3.0			6.0	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		5.0	20	μV/°C
Input Offset Current				20			30	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$		0.01	0.1				nA/°C
	$25°C \leq T_A \leq 70°C$					0.01	0.1	nA/°C
	$-55°C \leq T_A \leq 25°C$		0.02	0.2				nA/°C
	$0°C \leq T_A \leq 25°C$					0.02	0.2	nA/°C
Input Bias Current				100			300	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$		1.2	2.5				mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2K\Omega$	25			25			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10K\Omega$	±12	±14		±12	±14		V
	$R_L = 2K\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm 20V$	±15			±15			V
Common Mode Rejection Ratio	$R_S \leq 10K\Omega$	80	96		70	96		dB
Supply Voltage Rejection Ratio	$R_S \leq 10K\Omega$	80	96		70	96		dB

NOTES:

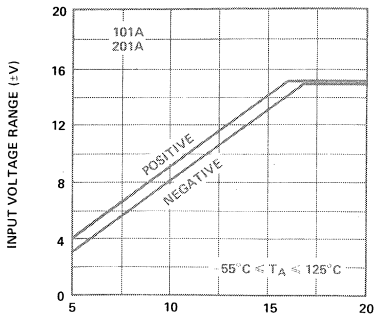
1. The maximum junction temperature of the 101A is 150°C, while that of the 201A and 301A is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Continuous short circuit is allowed for case temperatures to +125°C and ambient temperatures to +75°C. The limits for the 301A are 70°C case temperature and 55°C ambient temperature.
4. The specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the 201A, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$.

   Unless otherwise specified these specifications apply over the ambient temperature range of −55°C to +125°C for the 101A; −25°C to +85°C for the 201A; and 0°C to +70°C for the 301A. The applicable voltage range is $\pm 5V \leq V_S \leq \pm 20V$ for the 101A and 201A and $\pm 5V \leq V_S \leq 15V$ for the 301A.

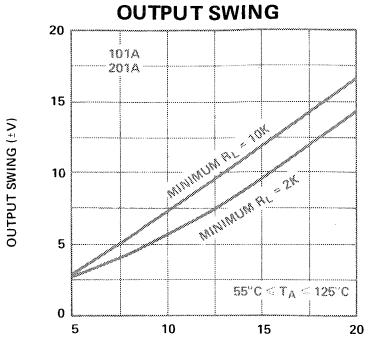
   C1 = 30pF.

Typical Characteristics

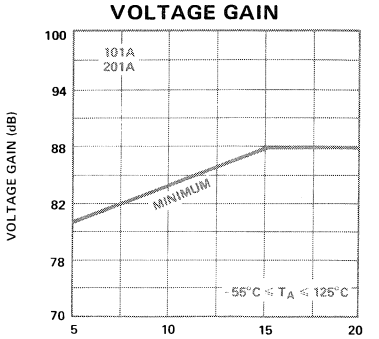
INPUT VOLTAGE GAIN



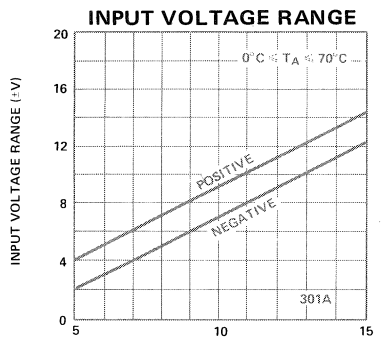
OUTPUT SWING



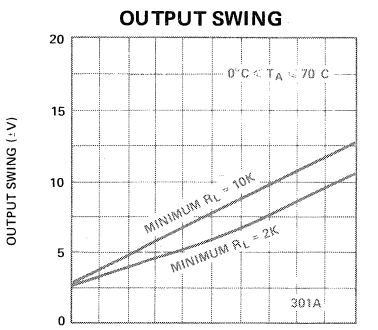
VOLTAGE GAIN



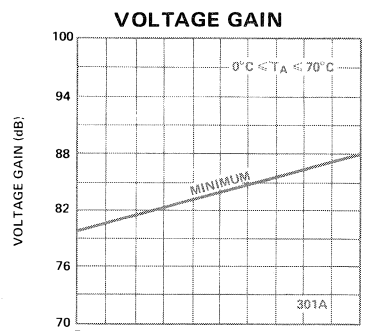
INPUT VOLTAGE RANGE



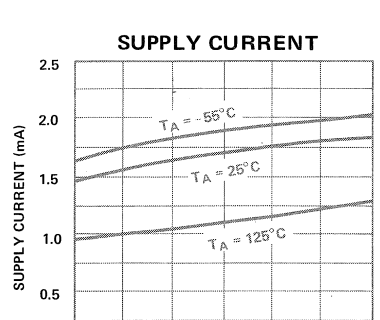
OUTPUT SWING



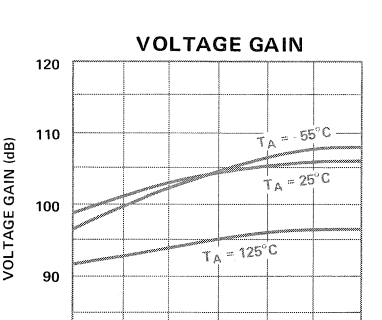
VOLTAGE GAIN



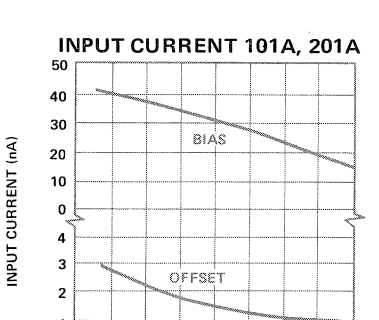
SUPPLY CURRENT



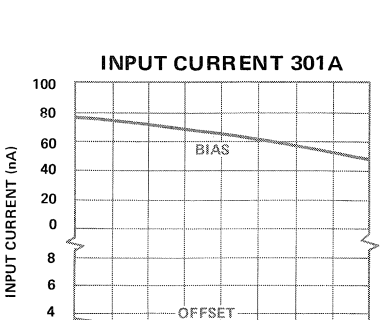
VOLTAGE GAIN



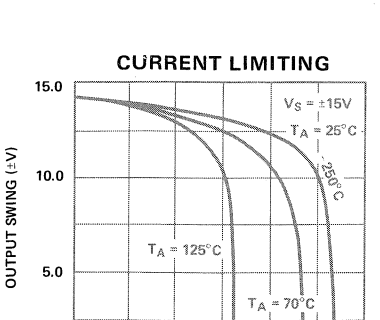
INPUT CURRENT 101A, 201A



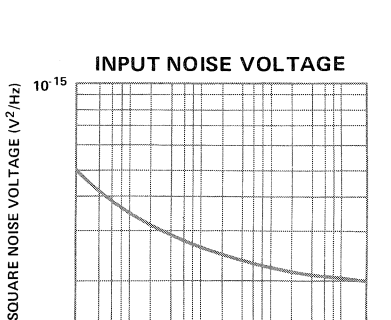
INPUT CURRENT 301A



CURRENT LIMITING

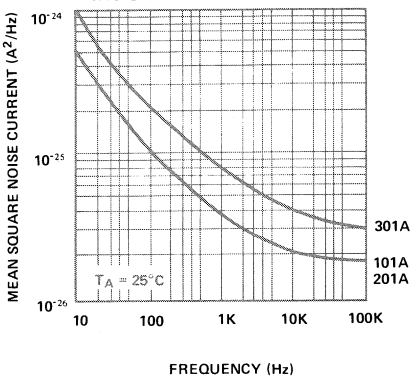


INPUT NOISE VOLTAGE

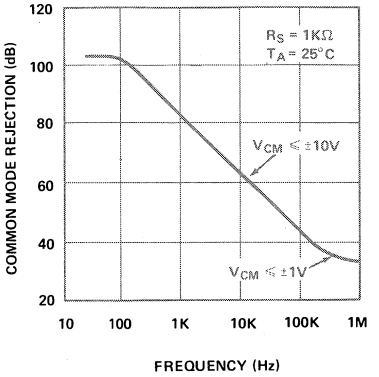


Typical Characteristics (Cont'd.)

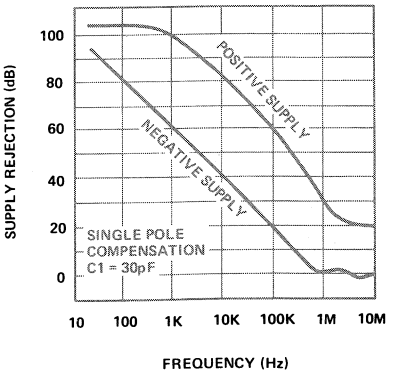
INPUT NOISE CURRENT



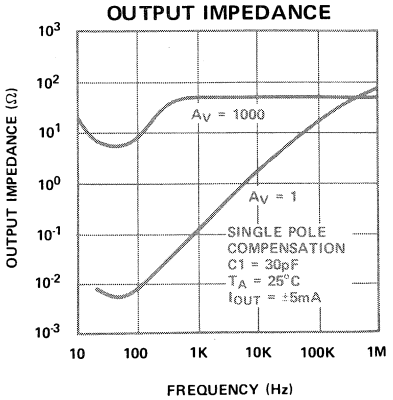
COMMON MODE REJECTION



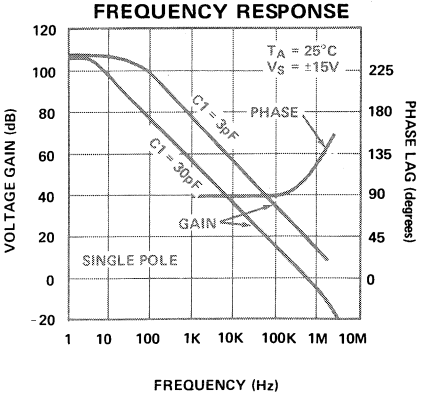
POWER SUPPLY REJECTION



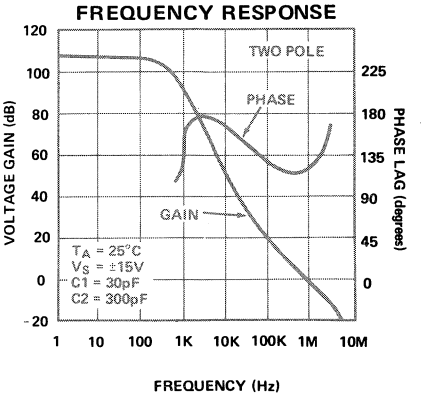
CLOSED LOOP
OUTPUT IMPEDANCE



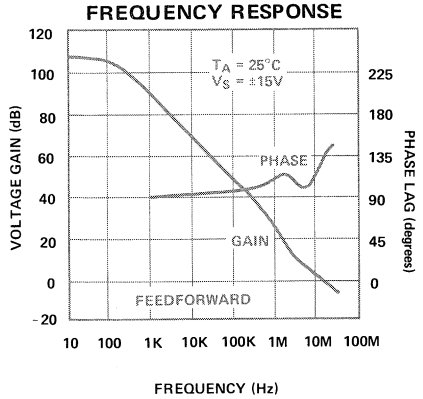
OPEN LOOP
FREQUENCY RESPONSE



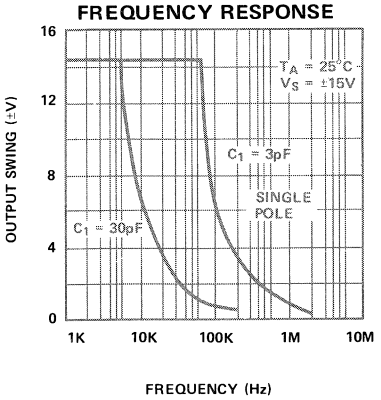
LARGE SIGNAL
FREQUENCY RESPONSE



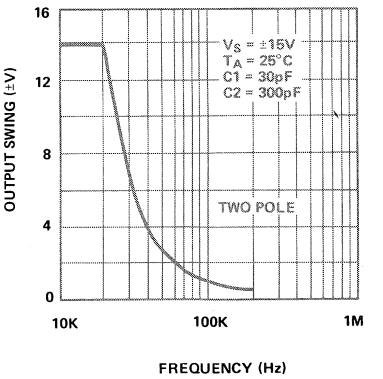
OPEN LOOP
FREQUENCY RESPONSE



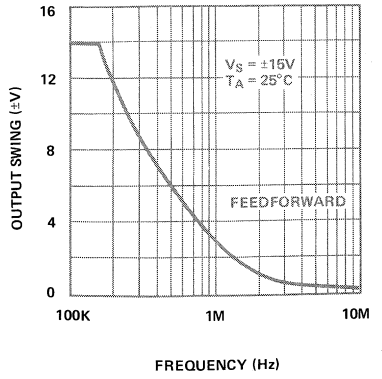
LARGE SIGNAL
FREQUENCY RESPONSE



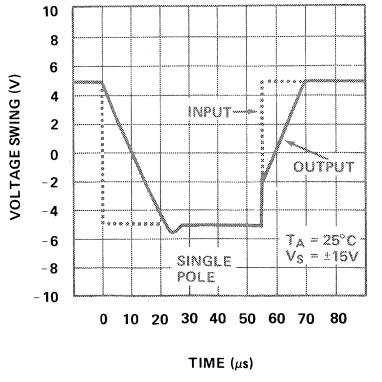
LARGE SIGNAL
FREQUENCY RESPONSE



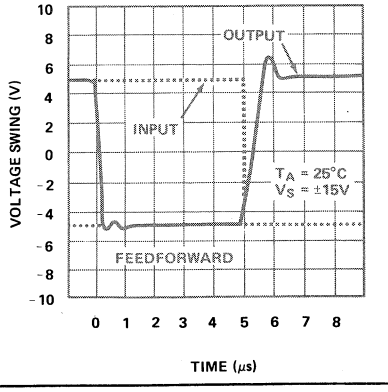
LARGE SIGNAL
FREQUENCY RESPONSE



VOLTAGE FOLLOWER
PULSE RESPONSE

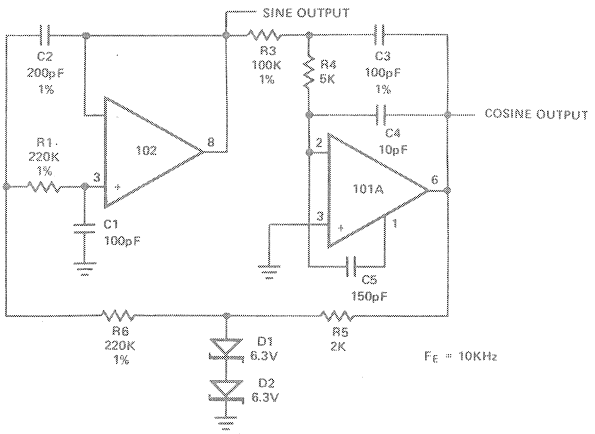


INVERTER
PULSE RESPONSE

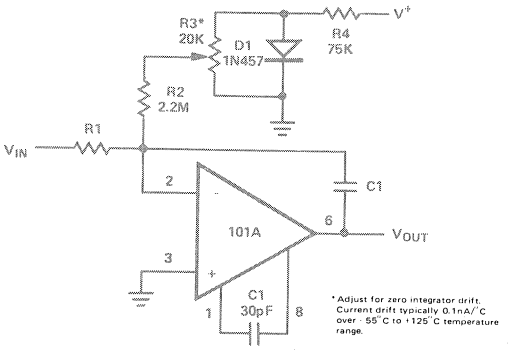


Typical Applications

SINE WAVE OSCILLATOR



INTEGRATOR WITH BIAS CURRENT COMPENSATION



Although the 101A is designed for trouble free operation, experience has indicated that it is wise to observe certain precautions given below to protect the devices from abnormal operating conditions. It might be pointed out that the advice given here is applicable to practically any IC op amp, although the exact reason why may differ with different devices.

When driving either input from a low-impedance source, a limiting resistor should be placed in series with the input lead to limit the peak instantaneous output current of the source to something less than 100mA. This is especially important when the inputs go outside a piece of equipment where they could accidentally be connected to high voltage sources. Large capacitors on the input (greater than 0.1μF) should be treated as a low source impedance and isolated with a resistor. Low impedance sources do not cause a problem unless their output voltage exceeds the supply voltage. However, the supplies go to zero when they are turned off, so the isolation is usually needed.

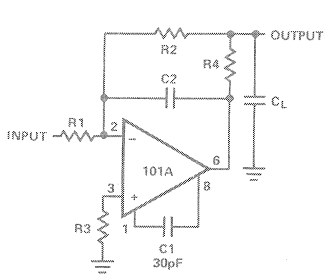
The output circuitry is protected against damage from shorts to ground. However, when the amplifier output is connected to a test point, it should be isolated by a limiting resistor, as test points frequently get shorted to bad places. Further, when the amplifier drives a load external to the equipment, it is also advisable to use some sort of limiting resistance to preclude mishaps.

Precautions should be taken to insure that the power supplies for the integrated circuit never become reversed—even under transient conditions. With reverse voltages greater than 1V, the IC will conduct excessive current, fuzing internal aluminum interconnects. If there is a possibility of this happening, clamp diodes with a high peak current rating should be installed on the supply lines. Reversal of the voltage between V^+ and V^- will always cause a problem, although reversals with respect to ground may also give difficulties in many circuits.

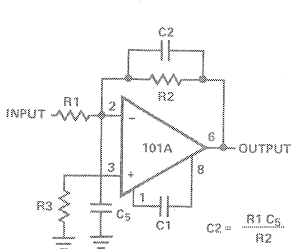
The minimum values given for the frequency compensation capacitor are stable only for source resistances less than 10KΩ, stray capacitances on the summing junction less than 5pF and capacitive loads smaller than 100pF. If any of these conditions are not met, it becomes necessary to overcompensate the amplifier with a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors or an RC network can be added to isolate capacitive loads.

Although the 101A is relatively unaffected by supply bypassing, this cannot be ignored altogether. Generally it is necessary to bypass the supplies to ground at least once on every circuit card, and more bypass points may be required if more than five amplifiers are used. When feed-forward compensation is employed, however, it is advisable to bypass the supply leads of each amplifier with low inductance capacitors because of the higher frequencies involved.

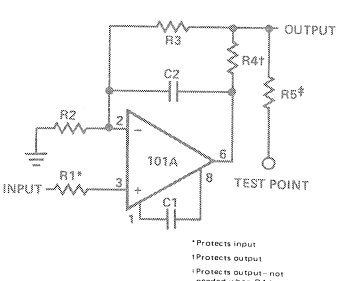
ISOLATING LARGE CAPACITIVE LOADS



COMPENSATING FOR STRAY INPUT CAPACITANCES OR LARGE FEEDBACK RESISTOR

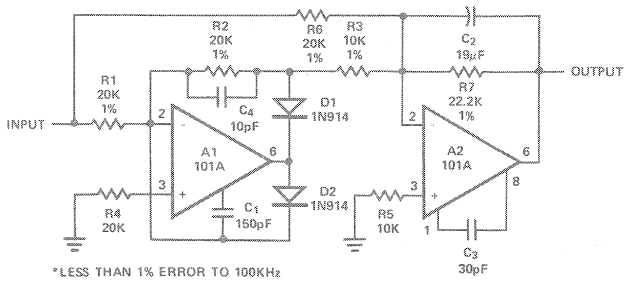


PROTECTING AGAINST GROSS FAULT CONDITIONS

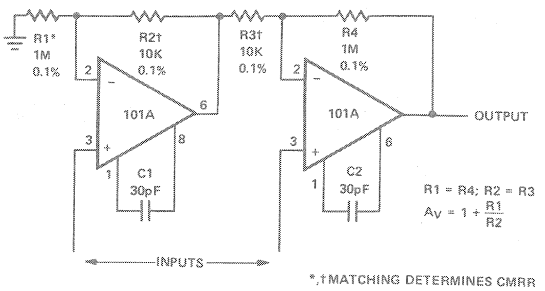


Typical Applications (Cont'd.)

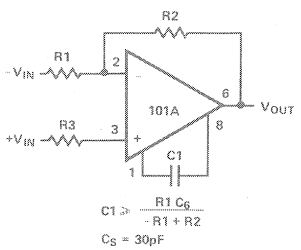
FAST AC/DC CONVERTER*



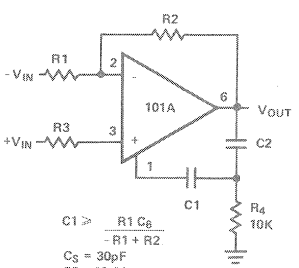
INSTRUMENTATION AMPLIFIER



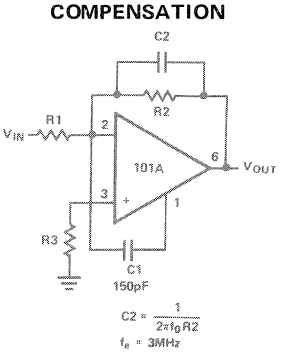
SINGLE POLE COMPENSATION



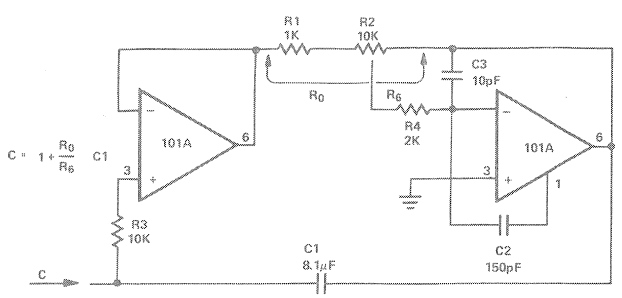
TWO POLE COMPENSATION



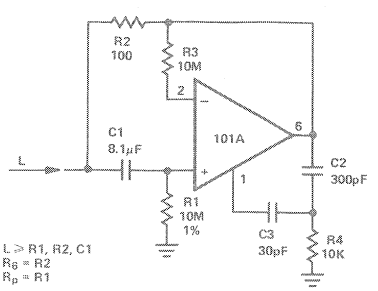
FEEDFORWARD COMPENSATION



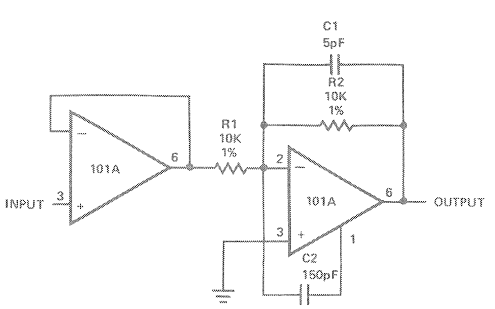
VARIABLE CAPACITANCE MULTIPLIER



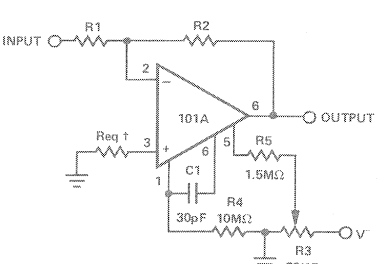
SIMULATED INDUCTOR



INVERTING AMPLIFIER WITH BALANCING CIRCUIT



FAST INVERTING AMPLIFIER WITH HIGH INPUT IMPEDANCE



107 Series

107•207•307

General Purpose Operational Amplifiers

Features

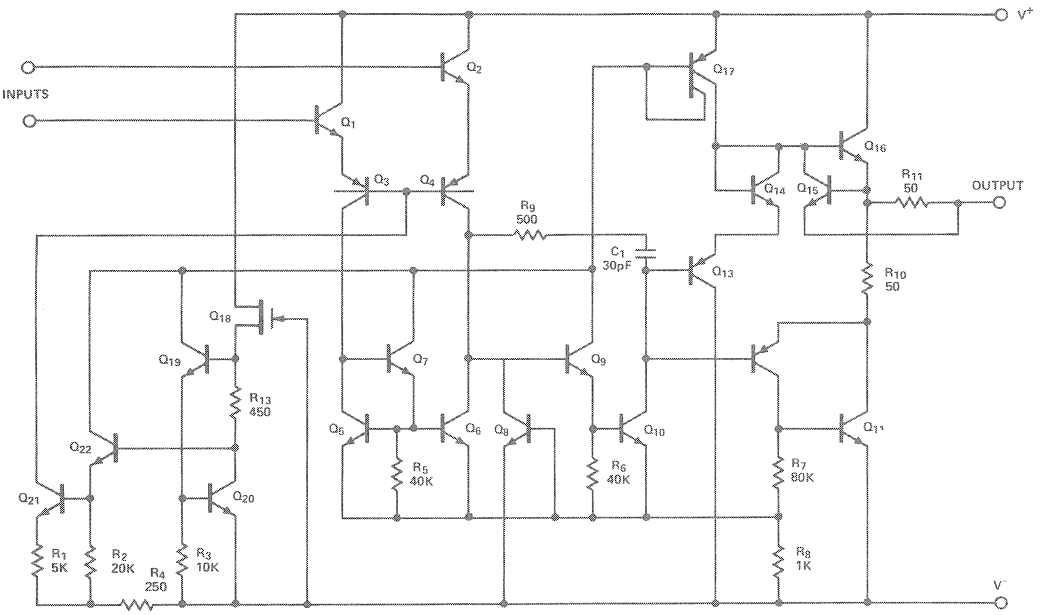
- LOW OFFSET VOLTAGE – 3mV MAX
- LOW INPUT CURRENT – 100nA MAX
- LOW OFFSET CURRENT – 20nA MAX
- OFFSETS GUARANTEED OVER ENTIRE COMMON MODE RANGE
- INTERNAL FREQUENCY COMPENSATION
- CONTINUOUS SHORT CIRCUIT PROTECTION

Description

The Teledyne Semiconductor 107 Series operational amplifiers are constructed on a single monolithic silicon substrate using planar epitaxial techniques. These high performance integrated circuits are intended for applications requiring low input offset voltage or low input offset current. The accuracy of long interval integrators, timers and sample and hold circuits is improved due to the low drift and low bias currents. Standard pin out allows direct replacement for the 709, 101, 101A, and the 141.

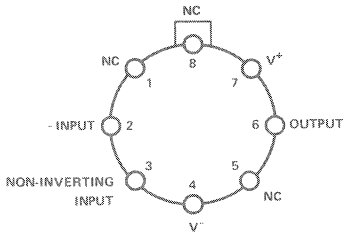
The 107 operates over a temperature range of −55°C to +125°C. The 307 operates from 0°C to +70°C. The 207 is the same as the 107 except its performance is guaranteed from −25°C to +85°C.

Equivalent Circuit Diagram



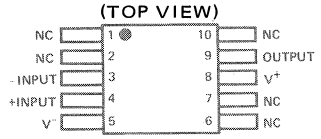
Connection Diagrams

E PACKAGE
8 LEAD METAL CAN
(TOP VIEW)



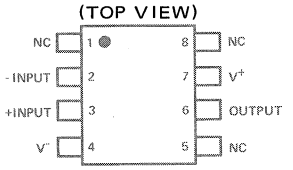
Order Part Numbers:
LM107H, LM207H,
LM307H

H PACKAGE
10 LEAD FLATPACK
(TOP VIEW)



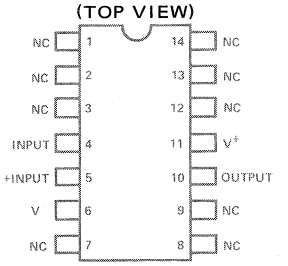
Order Part Number:
LM107F

P PACKAGE
8 LEAD MINIDIP
(TOP VIEW)



Order Part Number:
LM307N

L PACKAGE
14 LEAD CERDIP
(TOP VIEW)



Order Part Numbers:
LM107L, LM207L,
LM307L

Absolute Maximum Ratings

Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Output Short-Circuit Duration	
107, 207	Indefinite
307 (Note 2)	Indefinite
Supply Voltage	
107, 207	±22V
307	±18V
Power Dissipation (Note 3)	500mW
Operating Temperature Range	
107	−55°C/+125°C
207	−25°C/+85°C
307	0°C/+70°C
Storage Temperature Range	−65°C/+150°C
Lead Temperature (Soldering, 60 sec.)	300°C

Electrical Characteristics

PARAMETER	CONDITIONS	107/207			307			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50k\Omega$		0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		1.5	10		3	50	nA
Input Bias Current	$T_A = 25°C$		30	75		70	250	nA
Input Resistance	$T_A = 25°C$	1.5	4		0.5	2		MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 20V$ $T_A = 25°C$, $V_S = \pm 15V$		1.8	3.0		 1.8	 3.0	mA mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2K\Omega$	50	160		25	160		V/mV
Input Offset Voltage	$R_S \leq 50K\Omega$			3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		6.0	30	μV/°C
Input Offset Current				20			70	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$ $-55°C \leq T_A \leq 25°C$ $25°C \leq T_A \leq 70°C$ $0°C \leq T_A \leq 25°C$		0.01 0.02	0.1 0.2		 0.01 0.02	 0.3 0.6	nA/°C nA/°C nA/°C nA/°C
Input Bias Current				100			300	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$		1.2	2.5				mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10K\Omega$ $R_L = 2K\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Input Voltage Range	$V_S = \pm 20V$ $V_S = \pm 15V$	±15			 ±12			V V
Common Mode Rejection Ratio	$R_S \leq 50K\Omega$	80	96		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50K\Omega$	80	96		70	96		dB

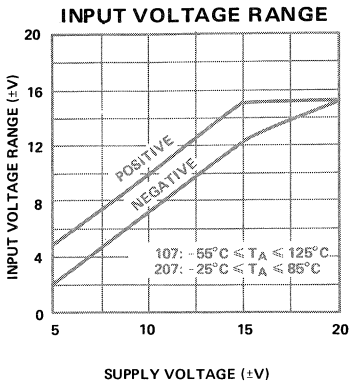
NOTES:

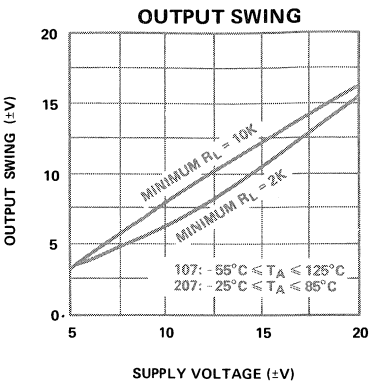
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Continuous short circuit is allowed for case temperatures to 70°C and ambient temperatures to 55°C.
3. 107 and 207: The maximum junction temperature of the 107 is 150°C, while that of the 207 is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

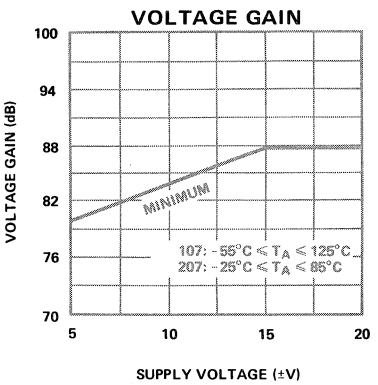
   307: For operating at elevated temperatures, the device must be derated based on a 100°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.
4. 107 and 207: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq 125°C$ for the 107 or $-25°C \leq T_A \leq 85°C$ for the 207, unless otherwise specified.
5. 307: The specifications apply for $0°C \leq T_A \leq 70°C$ and $\pm 5V \leq V_S \leq \pm 15V$, unless otherwise specified.

Guaranteed Performance Characteristics

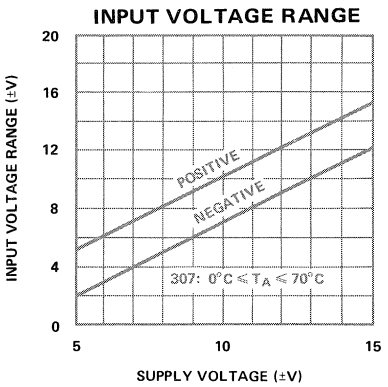
107•207

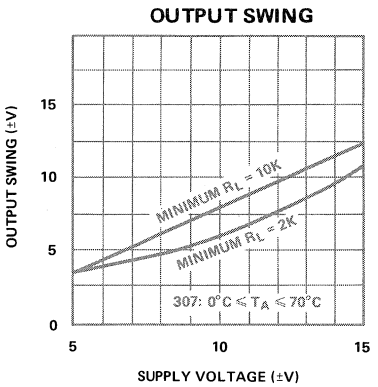


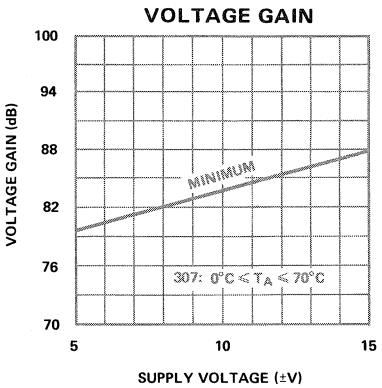




307

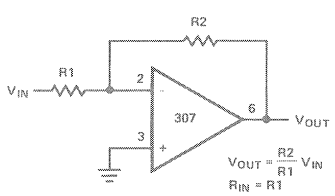




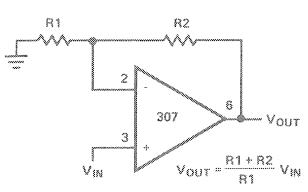


Typical Applications

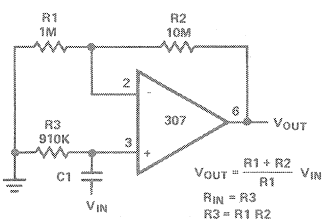
INVERTING AMPLIFIER



NON-INVERTING AMPLIFIER



NON-INVERTING AC AMPLIFIER



124 Series

124•224•324

Quad High Gain Operational Amplifiers

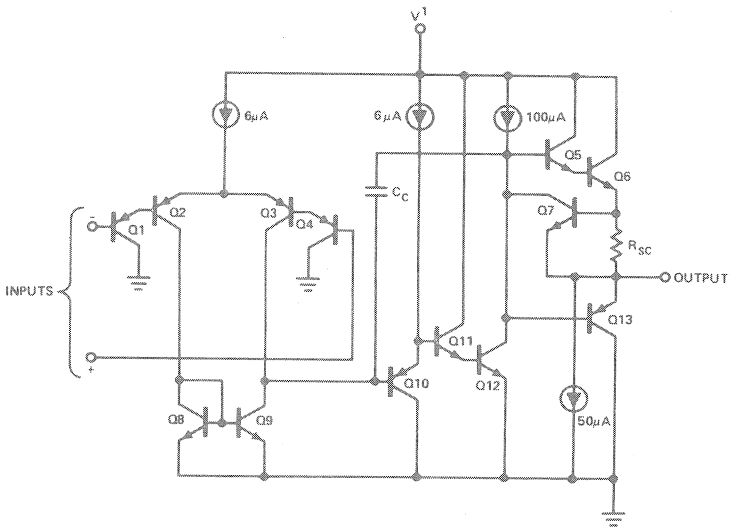
Features

- OUTPUT TTL, DTL COMPATIBLE
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- WIDE BANDWIDTH, TEMPERATURE COMPENSATED 1MHz
- VOLTAGE GAIN 100dB
- LARGE OUTPUT VOLTAGE SWING $0V_{DC}$ TO $V^+ - 1.5V_{OC}$

Description

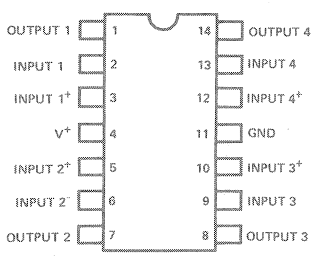
The 124/224/324 consists of four independent, high gain, internally frequency-compensated operational amplifiers designed specifically to operate from a single power over a wide range of voltages. Operation from split power supplies is also possible, and the low power supply current drain is independent of the magnitude of the power supply voltages. The 124 operates from −55°C to +125°C. The 224 is equal to the 324 over a temperature range of −25°C to +85°C. The 324 operates from 0°C to +70°C.

Equivalent Circuit Diagram



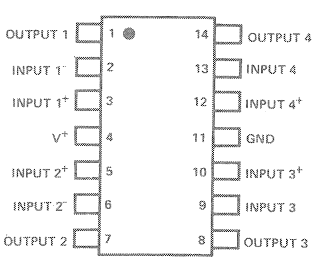
Connection Diagrams

L PACKAGE
14 LEAD CERDIP
(TOP VIEW)



Order Part Numbers:
LM124D, LM224D
LM324D,

J PACKAGE
14 LEAD PLASTIC DIP
(TOP VIEW)



Order Part Number:
LM324N

Absolute Maximum Ratings

Differential Input Voltage		$32V_{DC}$
Input Voltage		$-0.3V_{DC}$ to $+32V_{DC}$
Output Short-Circuit to GND (Note 1)		Continuous
$V^+ \leq 15V_{DC}$ and $T_A = 25°C$		
Supply Voltage, V^+		$32V_{DC}$ or $\pm 16V_{DC}$
Power Dissipation (Note 2)	Molded DIP	570mW
	Cavity DIP	900mW
Operating Temperature Range		
324		0°C to +70°C
224		−25°C to +85°C
124		−55°C to +125°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)		300°C

Electrical Characteristics ($V^+ = +5V_{DC}$ and $T_A = 25°C$ unless otherwise noted)

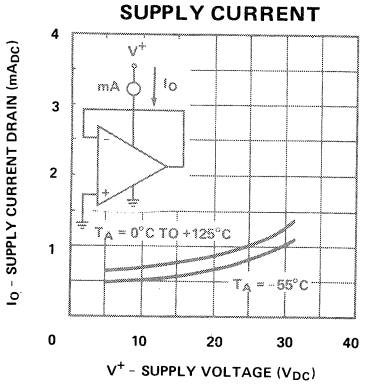
PARAMETER	CONDITIONS	124			224, 324			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S = 0\Omega$		2	5		2	7	mV_{DC}
Input Bias Current(3)	$I_{IN(+)}$ or $I_{IN(-)}$		45	300		45	500	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$		±3	±30		±5	±50	nA_{DC}
Input Common-Mode Voltage Range(4)		0		$V^+ - 1.5$	0		$V^+ - 1.5$	V_{DC}
Supply Current	$R_L = \infty$ On All Op Amps		0.8	2		0.8	2	mA_{DC}
Large Signal Voltage Gain	$R_L \geq 2K\Omega$		100			100		V/mV
Output Voltage Swing	$R_L = 2K\Omega$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V_{DC}
Common Mode Rejection Ratio	DC		85			85		dB
Power Supply Rejection Ratio	DC		100			100		dB
Amplifier-to-Amplifier Coupling	f = 1KHz to 20KHz (Input Referred)		−120			−120		dB
Output Current Source	$V_{IN}^+ = +1V_{OC}$, $V_{IN}^- = 0V_{DC}$	20	40		20	40		mA_{DC}
Output Current Sink	$V_{IN}^+ = +1V_{OC}$, $V_{IN}^- = 0V_{DC}$	10	20		10	20		mA_{DC}

NOTES:

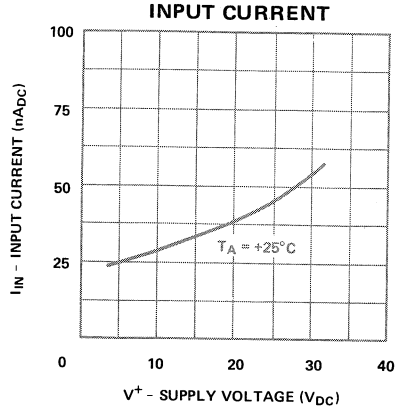
1. Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V^+. At values of supply voltage in excess of $+15V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
2. For operating at high temperatures, the 324 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The 224 and 124 can be derated based on a +150°C maximum junction temperature.
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
4. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to $+30V_{DC}$ without damage.

Typical Characteristics

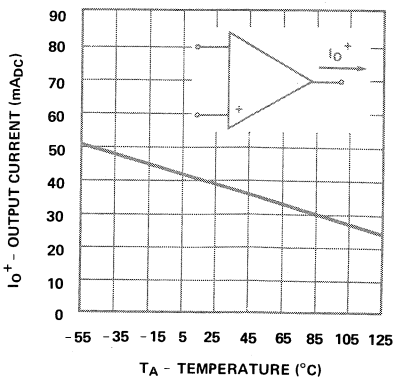
SUPPLY CURRENT



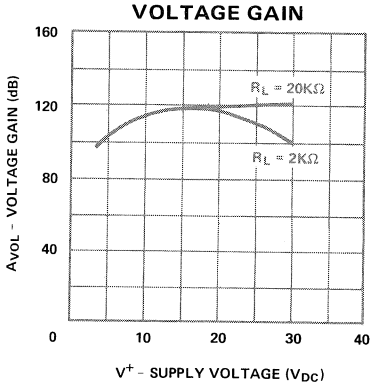
INPUT CURRENT



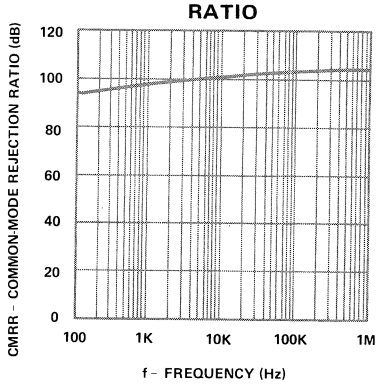
CURRENT LIMITING



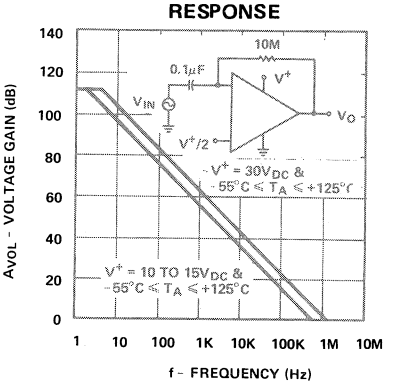
VOLTAGE GAIN



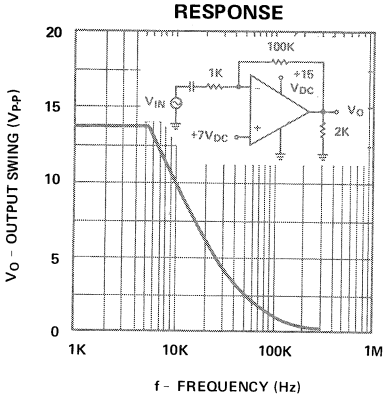
COMMON-MODE REJECTION RATIO



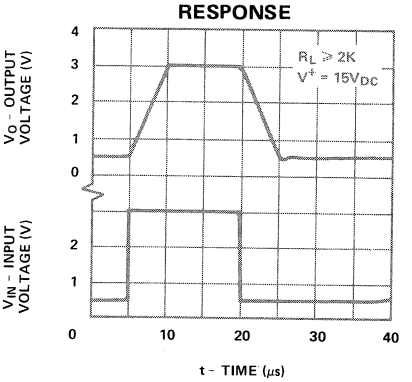
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE



VOLTAGE FOLLOWER PULSE RESPONSE



Typical Applications

The 124 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of OV_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of $2.3V_{DC}$.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative

Typical Applications (Cont'd.)

more than $-0.3V_{DC}$ (at 25°C). An input clamp consisting of a diode-connected NPN transistor (C-B short) can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class AB in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers.

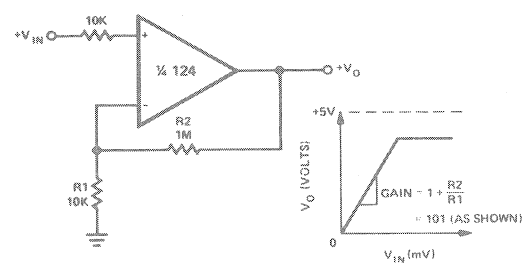
Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

The bias network of the 124 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from $3V_{DC}$ to $30V_{DC}$.

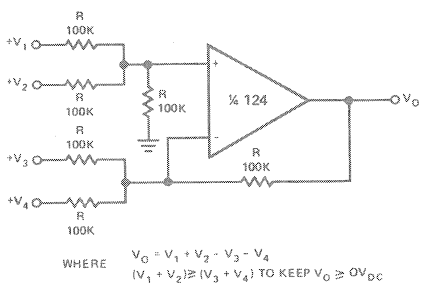
Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on "Typical Applications" emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

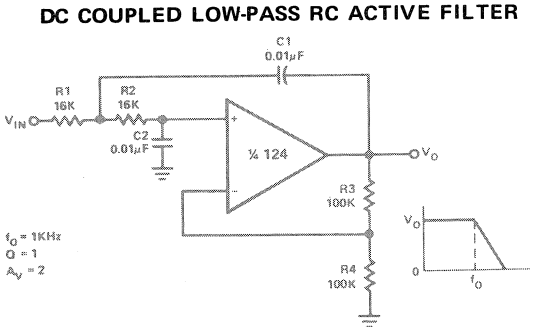
NON-INVERTING DC GAIN (0V INPUT = 0V OUTPUT)



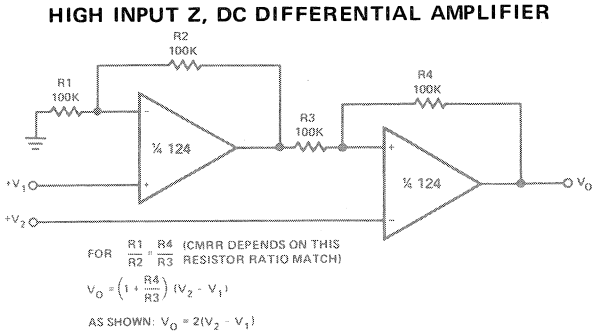
DC SUMMING AMPLIFIER
(V_{IN}'S ≥ 0V_{DC} AND V_O ≥ 0V_{DC})



DC COUPLED LOW-PASS RC ACTIVE FILTER

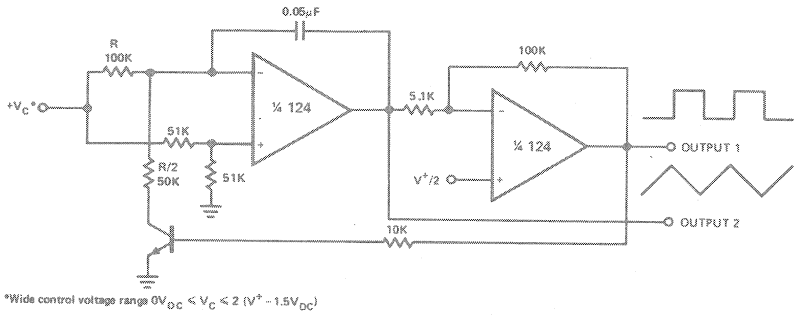


HIGH INPUT Z, DC DIFFERENTIAL AMPLIFIER



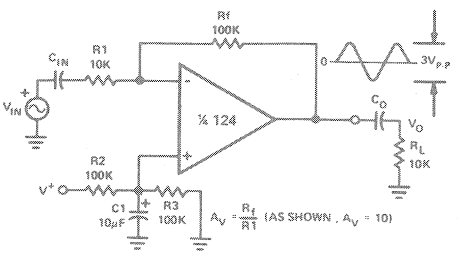
Typical Applications (Cont'd.)

VOLTAGE CONTROLLED OSCILLATOR (VCO)

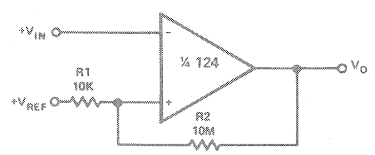


*Wide control voltage range $0V_{DC} \leq V_C \leq 2\ (V^+ - 1.5V_{DC})$

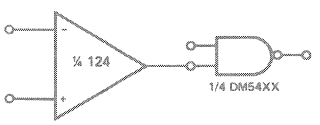
AC COUPLED INVERTING AMPLIFIER



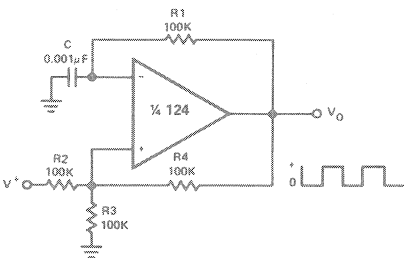
COMPARATOR WITH HYSTERESIS



DRIVING TTL



SQUAREWAVE OSCILLATOR



308/308A Series
Super Beta Operational Amplifiers

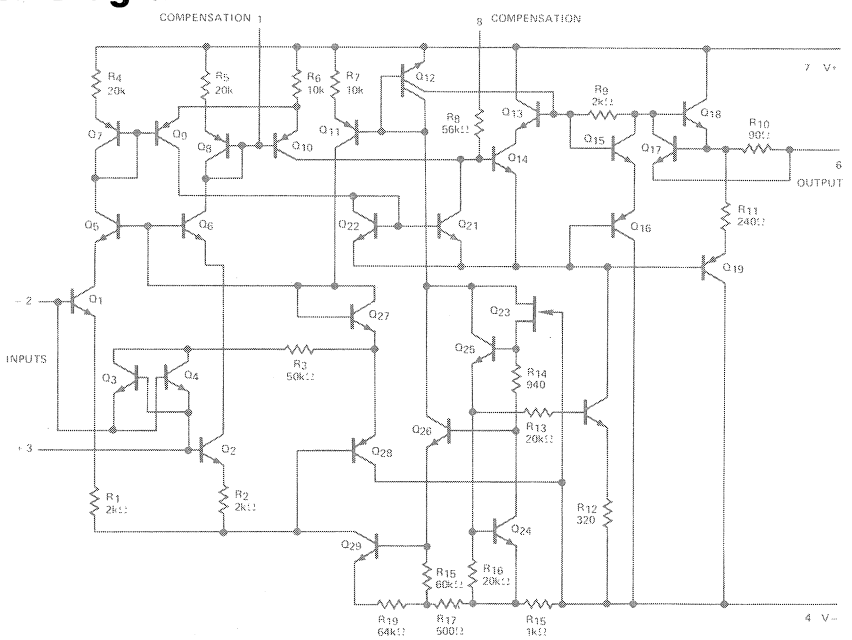
Features

- LOW OFFSET CURRENT OVER TEMPERATURE
- LOW INPUT BIAS CURRENT OVER TEMPERATURE
- LOW OFFSET VOLTAGE DRIFT
- LOW SUPPLY CURRENT
- OPERATION OVER WIDE SUPPLY RANGE

Description

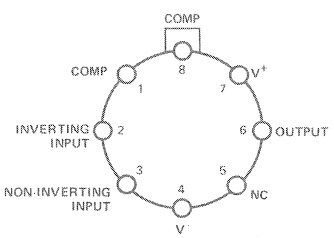
The Teledyne Semiconductor 308/308A are special purpose operational amplifiers constructed on a single monolithic silicon substrate using planar epitaxial techniques. High input impedance, low noise, input offsets, and temperature drift are made possible through use of super beta processing, making the device suitable for applications requiring high accuracy and low drift performance. The 308/308A is specially selected for extremely low offset voltage and drift, and high common mode rejection, making possible superior performance in applications where offset nulling is undesirable. Increased slew rate without performance compromise is available through use of feedforward compensation techniques, maximizing performance in high speed sample-and-hold circuits and precision high speed summing amplifiers. The wide supply range and excellent supply voltage rejection assure maximum flexibility in voltage follower, summing, and general feedback applications.

Equivalent Circuit Diagram



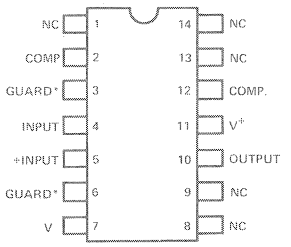
Connection Diagrams

E PACKAGE
8 LEAD METAL CAN
(TOP VIEW)



Order Part Numbers:
LM308AH,
LM308H

L PACKAGE
14 LEAD CERDIP
(TOP VIEW)



Order Part Numbers:
LM308AD,
LM308D

Absolute Maximum Ratings

Differential Input Current (Note 1)	±10mA
Input Voltage (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Indefinite
Supply Voltage	±18V
Internal Power Dissipation (Note 4)	500mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range Commercial	0°C to +70°C
Lead Temperature (Soldering, 60 Seconds)	300°C

NOTES:

1. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless adequate limiting resistance is used.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to either supply or ground. Rating applies to operation up to the maximum operating temperature range.
4. The maximum junction temperature of the 308/308A is 85°C. For operating at elevated temperatures, devices in the TO-99 package must be derated based on thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case.

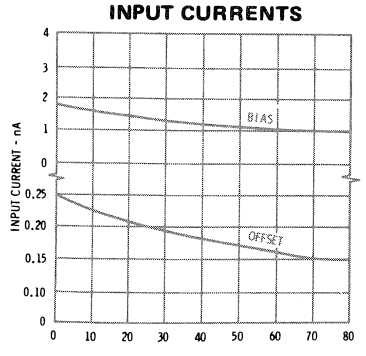
Electrical Characteristics

$\pm 5V \leqslant V_S \leqslant \pm 15V$, $T_A = 25°C$, $C_C = 30$ pF (Unless Otherwise Specified)

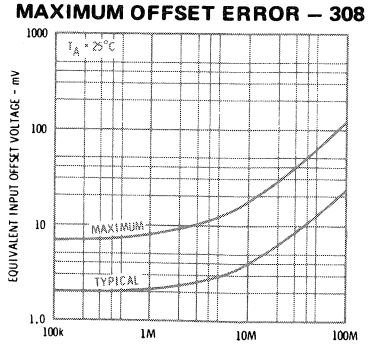
PARAMETER	CONDITIONS	308			308A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage			2.0	7.5		0.3	0.5	mV
Input Offset Current			0.2	1.0		0.2	1.0	nA
Input Bias Current			1.5	7.0		1.5	7.0	nA
Input Resistance		10	40		10	40		MΩ
Supply Current	$V_S = \pm 15V$		0.3	0.8		0.3	0.8	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $R_L \geqslant 10\ k\Omega$, $V_{OUT} = \pm 10V$	25,000	300,000		80,000	300,000		V/V
The following specifications apply for $0°C \leqslant T_A \leqslant +70°C$								
Input Offset Voltage				10			0.73	mV
Average Input Offset Voltage Drift			6.0	30		1.0	5.0	μV/°C
Input Offset Current				1.5			1.5	nA
Average Input Offset Current Drift			2.0	10		2.0	10	pA/°C
Input Bias Current				10			10	nA
Input Voltage Range	$V_S = \pm 15V$	±13.5			±13.5			V
Common Mode Rejection Ratio		80	100		96	110		dB
Supply Voltage Rejection Ratio		80	96		96	110		dB
Large Signal Voltage Gain	$V_S = \pm 15V$, $R_L \geqslant 10\ k\Omega$, $V_{OUT} = \pm 10V$	15,000			60,000			V/V
Output Voltage Swing	$V_S = \pm 15V$, $R_L \geqslant 10\ k\Omega$	±13	±14		±13	±14		V

Typical Performance

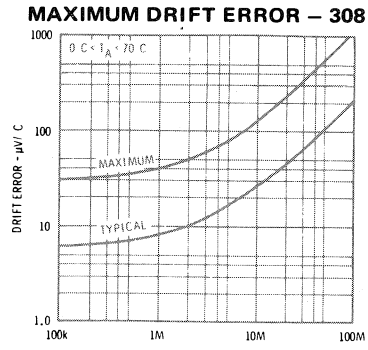
INPUT CURRENTS



MAXIMUM OFFSET ERROR – 308

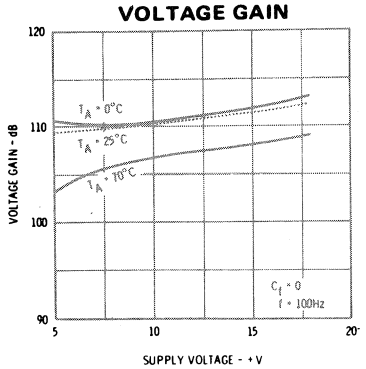


MAXIMUM DRIFT ERROR – 308

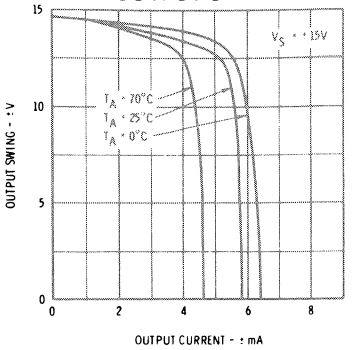


Typical Performance (Cont'd.)

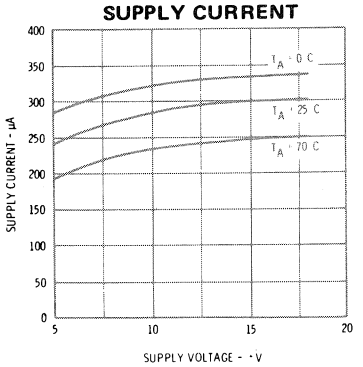
VOLTAGE GAIN



OUTPUT SWING



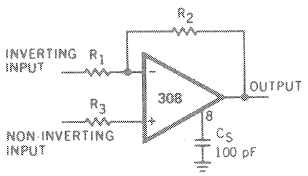
SUPPLY CURRENT

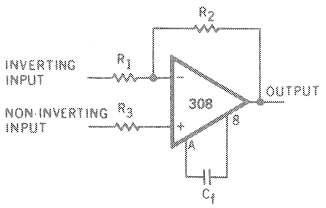


Typical Applications

Frequency Compensation Circuits

STANDARD COMPENSATION CIRCUITS

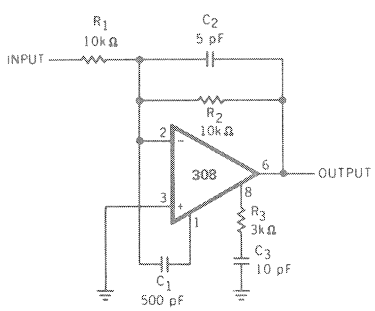




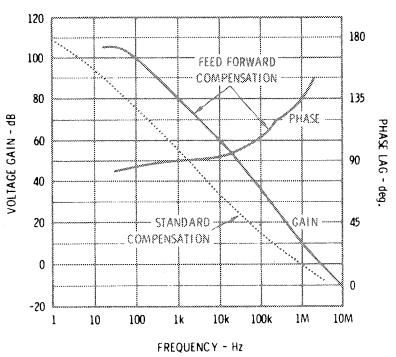
$$C_f \geq 30\left(\frac{1}{1+\frac{R_2}{R_1}}\right)$$

FEEDFORWARD COMPENSATION HIGHER SLEW RATES AND WIDER BANDWIDTH

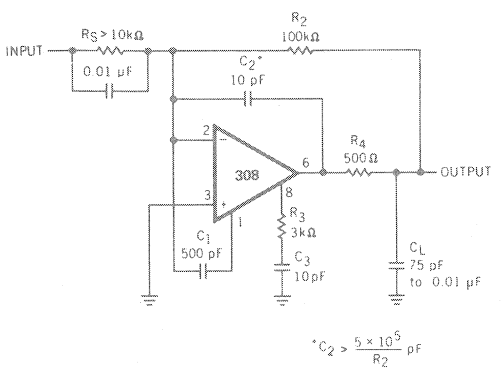
STANDARD FEEDFORWARD



OPEN LOOP VOLTAGE GAIN



FEEDFORWARD COMPENSATION FOR DECOUPLING LOAD CAPACITANCE



$$^*C_2 > \frac{5 \times 10^5}{R_2}\ \text{pF}$$

Application Hints

GUARDING

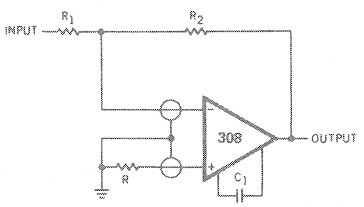
Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the 308 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at high temperatures, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high voltage pins are then absorbed by the guard.

Typical Applications (Cont'd.)

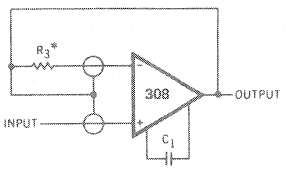
CONNECTION OF INPUT GUARDS

INVERTING AMPLIFIER



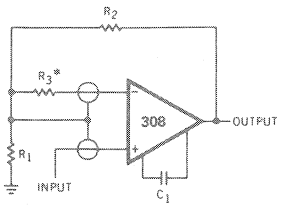
$$R = \frac{R_1 R_2}{R_1 + R_2}$$

FOLLOWER



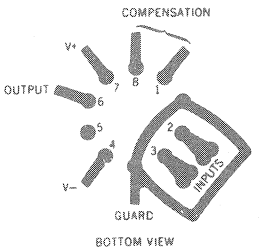
*Use to compensate for large source resistances.

NON-INVERTING AMPLIFIER

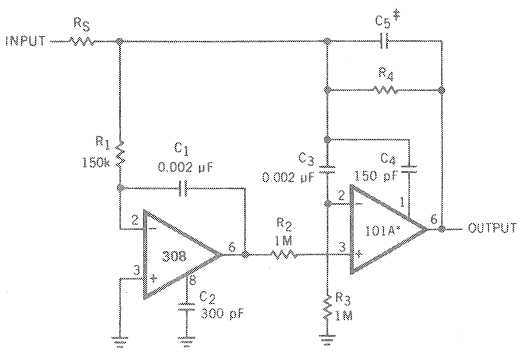


NOTE: $\frac{R_1 R_2}{R_1 + R_2}$ Must be low impedance

BOARD LAYOUT FOR INPUT GUARDING WITH TO–99 PACKAGE (BOTTOM VIEW)



FAST† SUMMING AMPLIFIER WITH LOW INPUT CURRENT

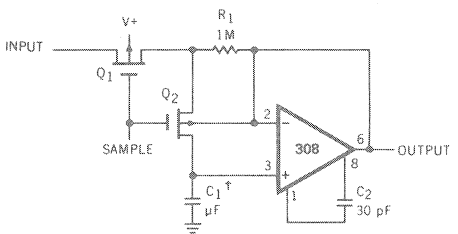


*In addition to increasing speed, the 101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

† Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10 V/µs

‡ $C_5 = \frac{6 \times 10^{-8}}{R_1}$

SAMPLE AND HOLD



* Worst case drift less than 2.5 mV/s
† Teflon, Polyethylene or Polycarbonate Dielectric Capacitor

709
Operational Amplifiers

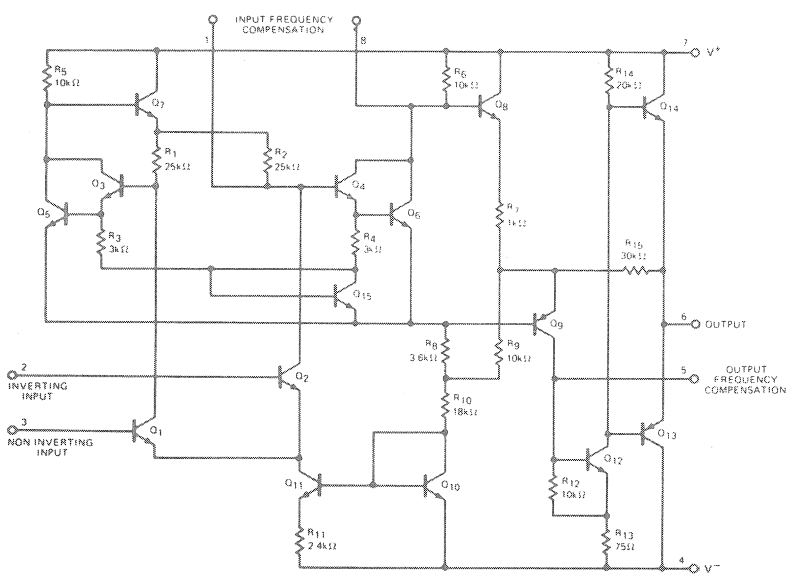
Features

- HIGH GAIN
- LOW VOLTAGE AND CURRENT OFFSETS – 2.0V AND 100mA TYP.
- HIGH INPUT IMPEDANCE – 250KΩ TYP.
- WIDE INPUT COMMON MODE RANGE
- HIGH OUTPUT SWING UNDER LOAD – ±14V
- LOW COST

Description

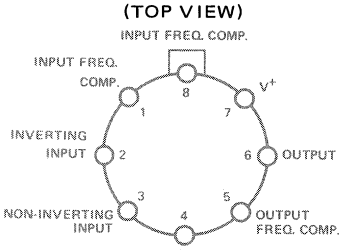
The Teledyne 709 is a low-cost, high-gain operational amplifier featuring low offset, high input impedance, large input common mode range, and high output swing under load. Excellent temperature stability and operation over a wide range of supply voltages make it useful in a wide variety of applications including dc servo systems, analog computers, and low-level instrumentation.

Equivalent Circuit Diagram



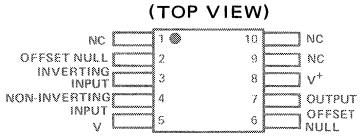
Connection Diagrams

E PACKAGE
8 LEAD METAL CAN
(TOP VIEW)



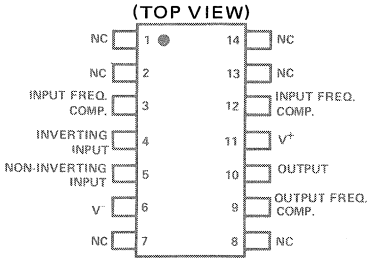
Order Part Numbers:
709AE (−55°C/+125°C)
709BE (−55°C/+125°C)
709CE (0°C/+70°C)

H PACKAGE
10 LEAD FLATPACK
(TOP VIEW)



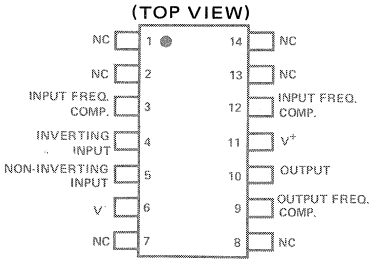
Order Part Numbers:
709AH (−55°C/+125°C)
709BH (−55°C/+125°C)

J PACKAGE
14 LEAD PLASTIC DIP
(TOP VIEW)



Order Part Numbers:
709CJ (0°C/+ 70°C)

N PACKAGE
14 LEAD CERDIP
(TOP VIEW)



Order Part Numbers:
709AN (−55°C/+125°C)
709BN (−55°C/+125°C)

Absolute Maximum Ratings

Differential Input Voltage	±5.0V
Input Voltage	±10V
Output Short Circuit Duration	5 sec.
Supply Voltage	±18V
Internal Power Dissipation (Note 1)	
Metal Can (E)	500mW
Ceramic Dual-In-Line (N)	670mW
Plastic Dual-In-Line (J)	530mW
Flatpack (H)	570mW
Operating Temperature Range	
Military (709A and 709B)	−55°C/+125°C
Commercial (709C)	0°C/+70°C
Storage Temperature Range	−65°C/+150°C
Lead Soldering Temperature (60 sec.)	300°C

NOTE:

1. Rating applies to ambient temperatures up to 75°C ambient. For operation above T_A = 75°C, derate linearly 6.7mW/°C for the metal can, 8.9mW/°C for the ceramic dual-in-line, and 7.5mW for the flatpack. For the flatpack, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch thick, epoxy-glass board with ten 0.03-inch wide, 2 oz. copper conductors.

Electrical Characteristics (T_A = +25°C, ±9 V ≤ V_S ≤ ±15 V unless otherwise specified)

709A

PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage		$R_S \leq 10\ k\Omega$		0.6	2.0	mV
Input Offset Current				10	50	nA
Input Bias Current				100	200	nA
Input Resistance			350	700		kΩ
Output Resistance				150		Ω
Supply Current		V_S = ±15 V		2.5	3.6	mA
Power Consumption		V_S = ±15 V		75	108	mW
Transient Response	Risetime	V_S = ±15 V, V_{IN} = 20 mV, R_L = 2 kΩ, C_1 = 5 nF, R_1 = 1.5 kΩ, C_2 = 200 pF, R_2 = 50Ω $C_L \leq 100$ pF			1.5	μs
	Overshoot				30	%
The following specifications apply for −55°C ≤ T_A ≤ +125°C:						
Input Offset Voltage		$R_S \leq 10\ k\Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage		R_S = 50Ω, T_A = +25°C to +125°C		1.8	10	μV/°C
		R_S = 50Ω, T_A = +25°C to −55°C		1.8	10	μV/°C
		R_S = 10 kΩ, T_A = +25°C to +125°C		2.0	15	μV/°C
		R_S = 10 kΩ, T_A = +25°C to −55°C		4.8	25	μV/°C
Input Offset Current		T_A = +125°C		3.5	50	nA
		T_A = −55°C		40	250	nA
Average Temperature Coefficient of Input Offset Current		T_A = +25°C to +125°C		0.08	0.5	nA/°C
		T_A = +25°C to −55°C		0.45	2.8	nA/°C
Input Bias Current		T_A = −55°C		300	600	nA
Input Resistance		T_A = −55°C	85	170		kΩ
Input Voltage Range		V_S = ±15 V	±8.0			V
Common Mode Rejection Ratio		$R_S \leq 10\ k\Omega$	80	110		dB
Supply Voltage Rejection Ratio		$R_S \leq 10\ k\Omega$		40	100	μV/V
Large Signal Voltage Gain		V_S = ±15 V, $R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	25,000		70,000	V/V
Output Voltage Swing		V_S = ±15 V, $R_L \geq 10\ k\Omega$	±12	±14		V
		V_S = ±15 V, $R_L \geq 2\ k\Omega$	±10	±13		V
Supply Current		T_A = +125°C, V_S = ±15 V		2.1	3.0	mA
		T_A = −55°C, V_S = ±15 V		2.7	4.5	mA
Power Consumption		T_A = +125°C, V_S = ±15 V		63	90	mW
		T_A = −55°C, V_S = ±15 V		81	135	mW

Electrical Characteristics (T_A = +25°C, ±9 V ≤ V_S ≤ ±15 V unless otherwise specified)

709B

PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage		R_S ≤ 10 kΩ		1.0	5.0	mV
Input Offset Current				50	200	nA
Input Bias Current				200	500	nA
Input Resistance			150	400		kΩ
Output Resistance				150		Ω
Power Consumption		V_S = ±15 V		80	165	mW
Transient Response	Risetime	V_{IN} = 20 mV, R_L = 2 kΩ, C_1 = 5000 pF, R_1 = 1.5 kΩ, C_2 = 200 pF, R_2 = 50Ω		0.3	1.0	μs
	Overshoot	C_L ≤ 100 pF		10	30	%
The following specifications apply for –55°C ≤ T_A ≤ +125°C:						
Input Offset Voltage		R_S ≤ 10 kΩ			6.0	mV
Average Temperature Coefficient of Input Offset Voltage		R_S = 50Ω		3.0		μV/°C
		R_S ≤ 10 kΩ		6.0		μV/°C
Large Signal Voltage Gain		V_S = ±15 V, R_L ≥ 2 kΩ, V_{OUT} = ±10 V	25,000	45,000	70,000	V/V
Output Voltage Swing		V_S = ±15 V, R_L ≥ 10 kΩ	±12	±14		V
		V_S = ±15 V, R_L ≥ 2 kΩ	±10	±13		V
Input Voltage Range		V_S = ±15 V	±8.0	±10		V
Common Mode Rejection Ratio		R_S ≤ 10 kΩ	70	90		dB
Supply Voltage Rejection Ratio		R_S ≤ 10 kΩ		25	150	μV/V
Input Offset Current		T_A = +125°C		20	200	nA
		T_A = –55°C		100	500	nA
Input Bias Current		T_A = –55°C		0.5	1.5	μA
Input Resistance			40	100		kΩ

Electrical Characteristics (V_S = ±15 V, T_A = 25°C unless otherwise specified)

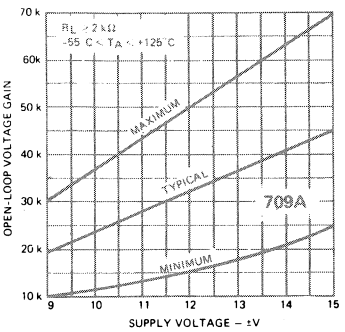
709C

PARAMETER		CONDITIONS	MIN.	MAX.	TYP.	UNITS
Input Offset Voltage		R_S ≤ 10 kΩ, ±9 V ≤ V_S ≤ ±15 V		2.0	7.5	mV
Input Offset Current				100	500	nA
Input Bias Current				0.3	1.5	μA
Input Resistance			50	250		kΩ
Output Resistance				150		Ω
Large Signal Voltage Gain		R_L ≥ 2 kΩ, V_{OUT} = ±10 V	15,000	45,000		V/V
Output Voltage Swing		R_L ≥ 10 kΩ	±12	±14		V
		R_L ≥ 2 kΩ	±10	±13		V
Input Voltage Range			±8.0	±10		V
Common Mode Rejection Ratio		R_S ≤ 10 kΩ	65	90		dB
Supply Voltage Rejection Ratio		R_S ≤ 10 kΩ		25	200	μV/V
Power Consumption				80	200	mW
Transient Response	Risetime	V_{IN} = 20 mV, R_L = 2 kΩ, C_1 = 5000 pF, R_1 = 1.5 kΩ, C_2 = 200 pF, R_2 = 50Ω		0.3		μs
	Overshoot	C_L ≤ 100 pF		10		%
The following specifications apply for 0°C ≤ T_A ≤ +70°C:						
Input Offset Voltage		R_S ≤ 10 kΩ, ±9 V ≤ V_S ≤ ±15 V			10	mV
Input Offset Current					750	nA
Input Bias Current					2.0	μA
Large Signal Voltage Gain		R_L ≥ 2 kΩ, V_{OUT} = ±10 V	12,000			V/V
Input Resistance			35			kΩ

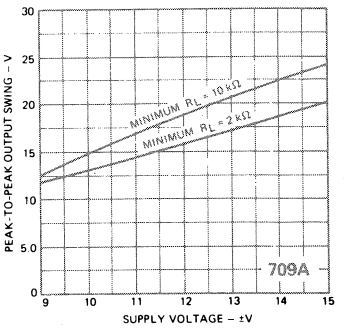
Typical Characteristics

709A

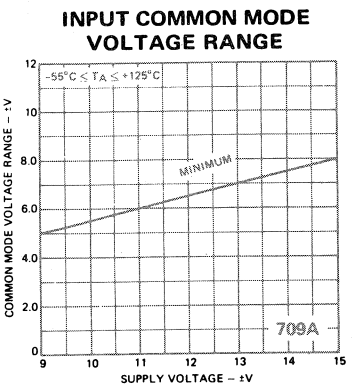
VOLTAGE GAIN



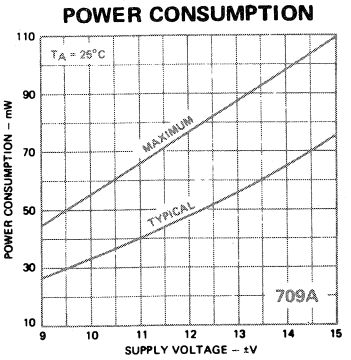
OUTPUT VOLTAGE SWING



INPUT COMMON MODE VOLTAGE RANGE

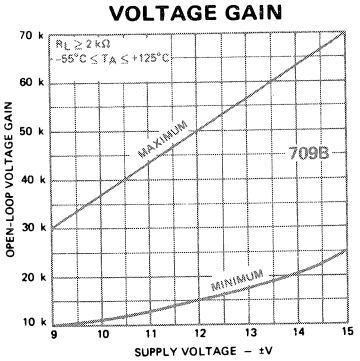


POWER CONSUMPTION

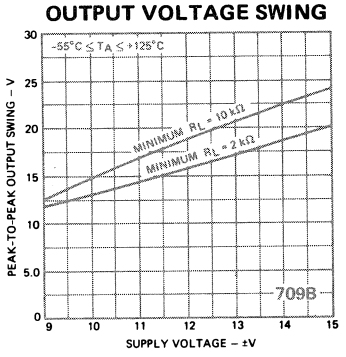


709B

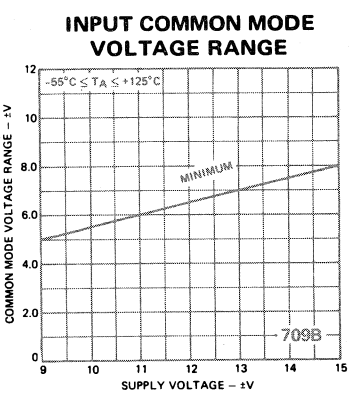
VOLTAGE GAIN



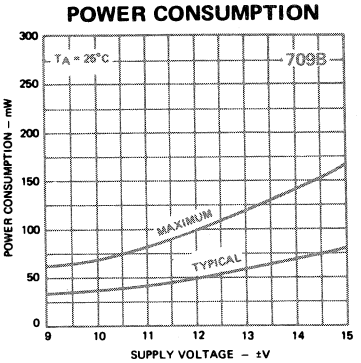
OUTPUT VOLTAGE SWING



INPUT COMMON MODE VOLTAGE RANGE

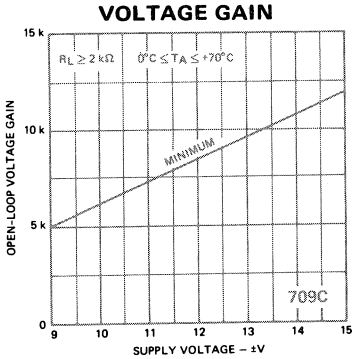


POWER CONSUMPTION

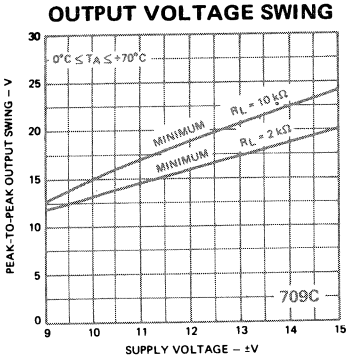


709C

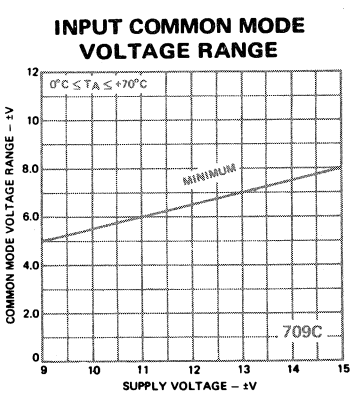
VOLTAGE GAIN



OUTPUT VOLTAGE SWING

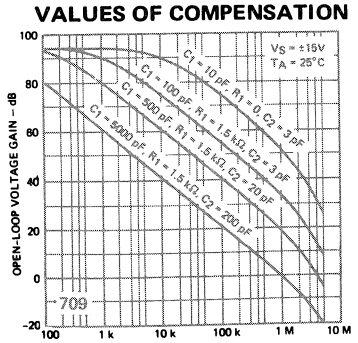


INPUT COMMON MODE VOLTAGE RANGE

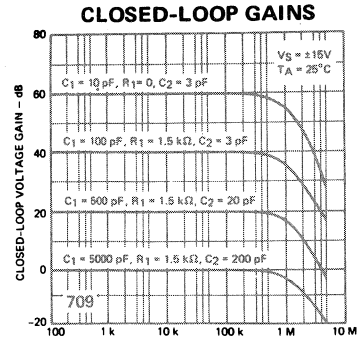


FREQUENCY COMPENSATION CURVES FOR ALL TYPES

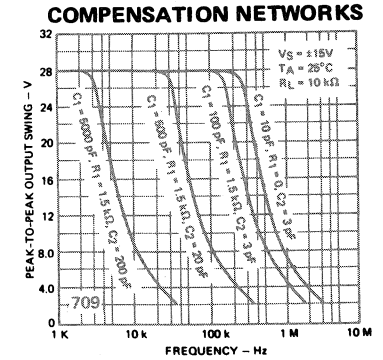
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS

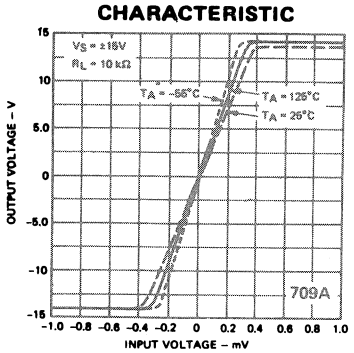


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS

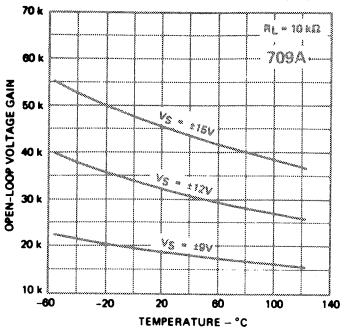


Typical Characteristics (Cont'd.)

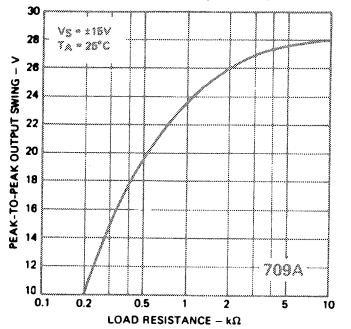
VOLTAGE TRANSFER CHARACTERISTIC



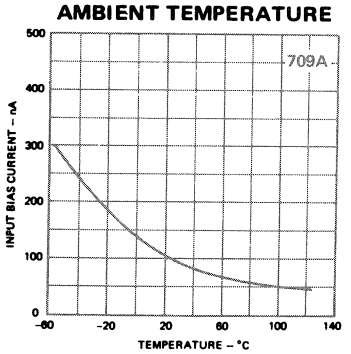
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



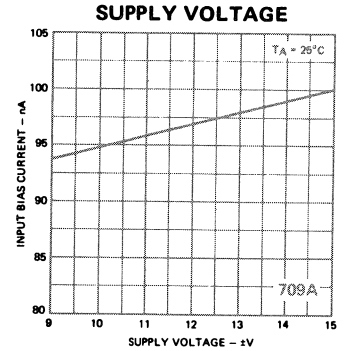
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



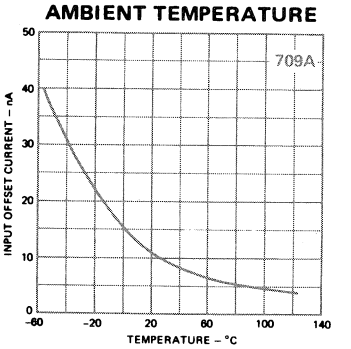
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



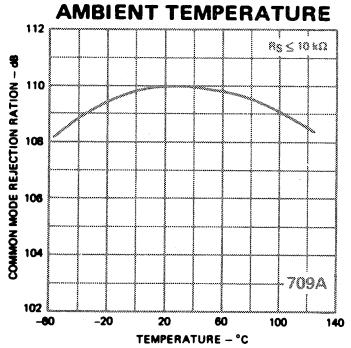
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



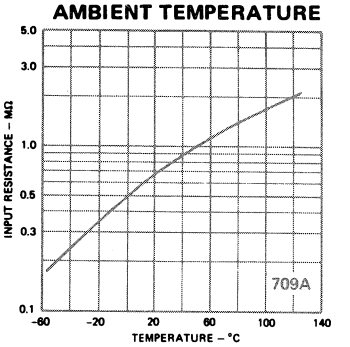
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



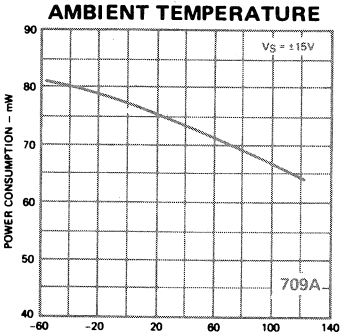
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



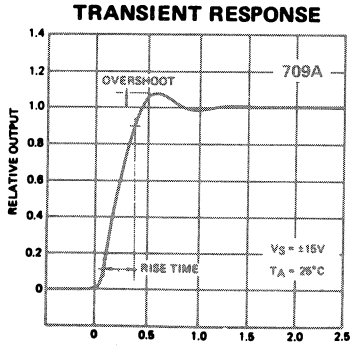
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



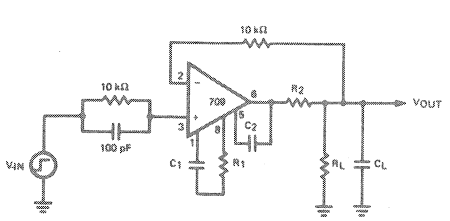
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



TRANSIENT RESPONSE

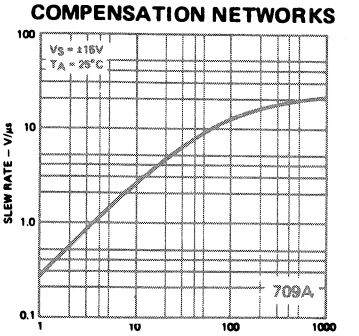


TRANSIENT RESPONSE TEST CIRCUIT



Pin numbers only apply to metal can package.

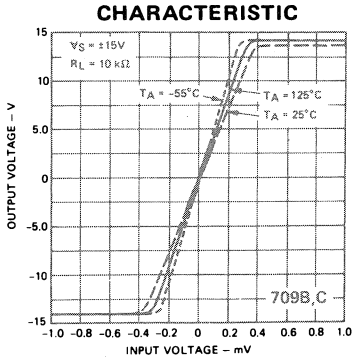
SLEW RATE AS A FUNCTION OF CLOSED-LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS



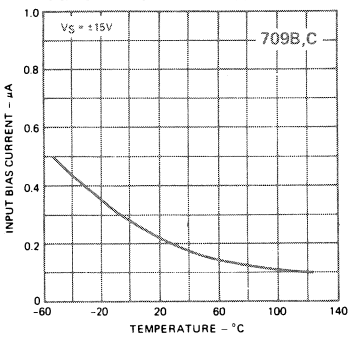
Typical Characteristics (Cont'd.)

709B AND 709C

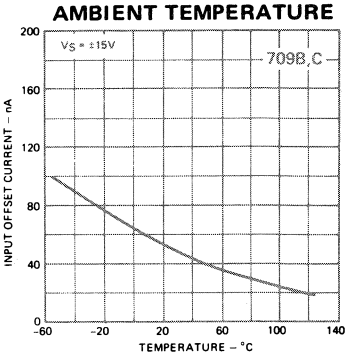
VOLTAGE TRANSFER CHARACTERISTIC



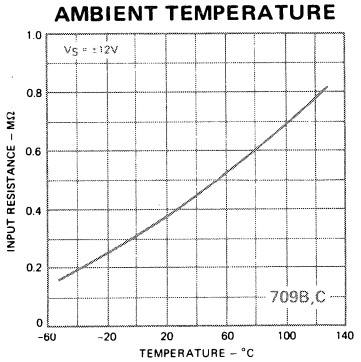
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



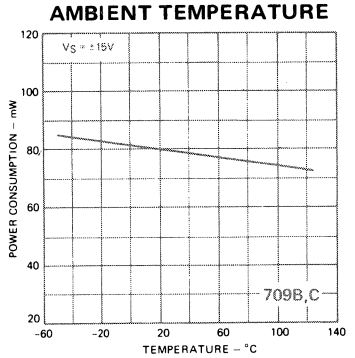
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



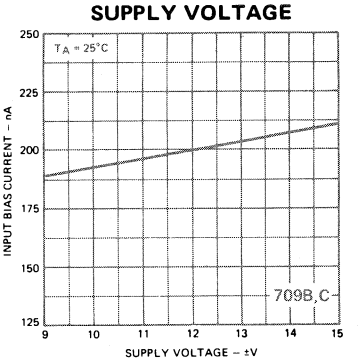
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



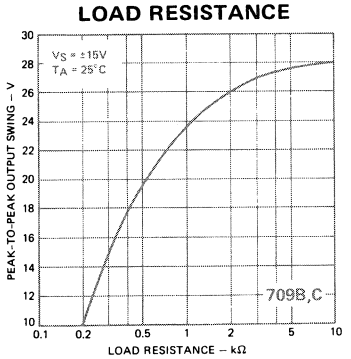
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



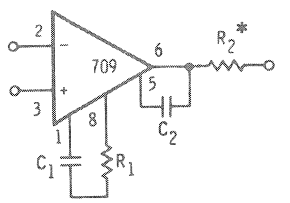
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

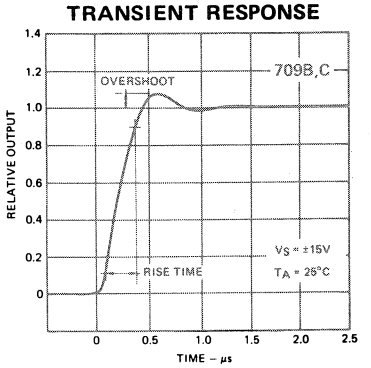


FREQUENCY COMPENSATION CIRCUIT



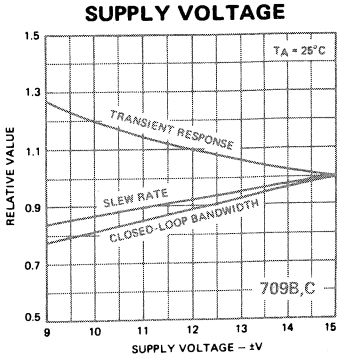
* Use R_2 = 50 Ω when the amplifier is operated with capacitive loading.

TRANSIENT RESPONSE

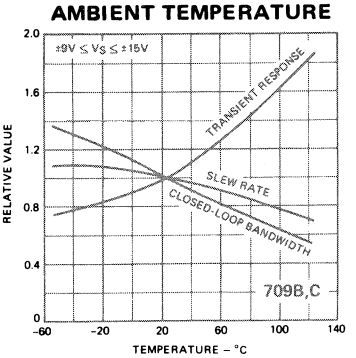


709B AND 709C

FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE

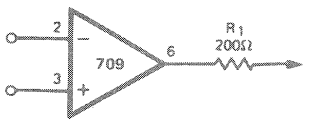


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

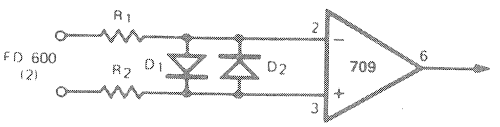


Typical Applications

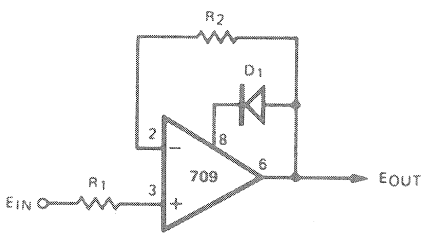
OUTPUT SHORT-CIRCUIT PROTECTION



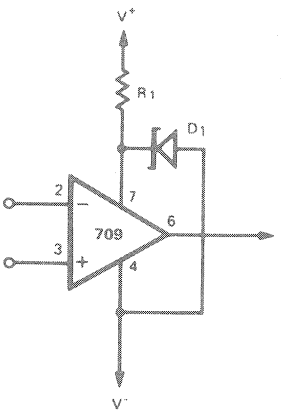
INPUT BREAKDOWN PROTECTION



LATCH-UP PROTECTION



SUPPLY OVERVOLTAGE PROTECTION



Pin numbers only apply to metal can package.

741
Operational Amplifiers

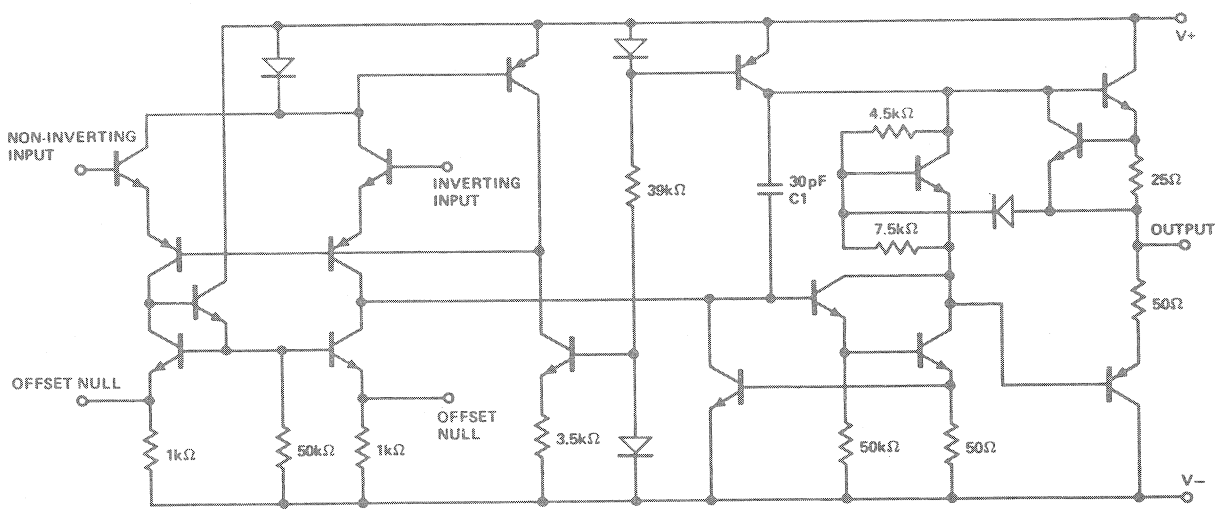
Features

- INTERNAL COMPENSATION ELIMINATES EXTERNAL COMPENSATION COMPONENTS
- OUTPUT SHORT CIRCUIT PROTECTION
- OFFSET NULL CAPABILITY
- LOW POWER CONSUMPTION
- LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES

Description

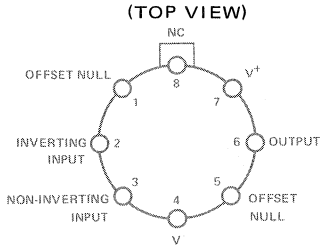
The Teledyne Semiconductor 741 Operational Amplifier is constructed on a single monolithic silicon substrate using planar epitaxial techniques. The incorporation of a MOS capacitor directly on the substrate eliminates the need for external compensation. Input overvoltage and output short circuit protection coupled with the elimination of latch up problems result in an excellent general purpose amplifier. Proper pin arrangement makes the 741 a direct replacement for the 709 and 101A operational amplifiers for most applications with the resultant elimination of compensation components.

Equivalent Circuit Diagram



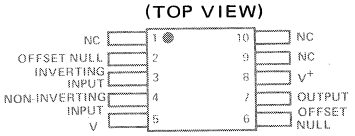
Connection Diagrams

E PACKAGE
8 LEAD METAL CAN
(TOP VIEW)



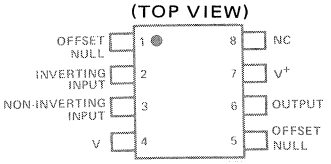
Order Part Numbers:
741BE, 741CE

H PACKAGE
10 LEAD FLATPACK
(TOP VIEW)



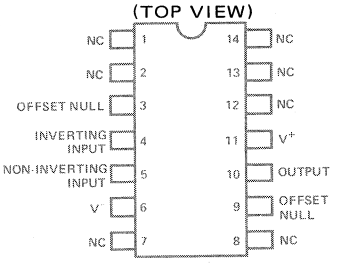
Order Part Number:
741BH

P PACKAGE
8 LEAD MINIDIP
(TOP VIEW)



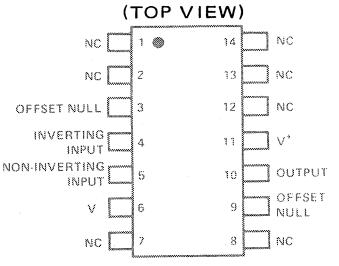
Order Part Number:
741CP

L PACKAGE
14 LEAD CERDIP
(TOP VIEW)



Order Part Numbers:
741BL, 741CL

J PACKAGE
14 LEAD PLASTIC DIP
(TOP VIEW)



Order Part Number:
741CJ

Absolute Maximum Ratings

	741B	741C
Input Voltage (Note 1)	±15V	±15V
Differential Input Voltage	±30V	±30V
Output Short Circuit Duration (Note 2)	Indefinite	Indefinite
Internal Power Dissipation (Note 3)		
Metal Can (E)	500mW	500mW
Ceramic Dual-In-Line (L)	670mW	670mW
Flatpack (H)	570mW	570mW
Storage Temperature Range	−65°C/+150°C	−65°C/+150°C
Operating Temperature Range	−55°C/+125°C	0°C/+70°C
Lead Soldering Temperature (60 sec.)	300°C	300°C
Junction Temperature	150°C	150°C

The above ratings are not meant to imply operation at each of these extremes simultaneously. Exceeding any or all of the absolute maximum ratings may cause permanent damage to the device.

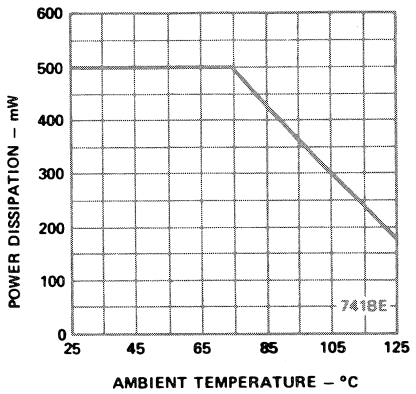
NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
3. Rating applies to ambient temperatures up to 75°C ambient. For operation above T_A = 75°C, derate linearly 6.7mW/°C for the metal can, 8.9mW/°C for the ceramic dual-in-line, and 7.5mW/°C for the flatpack. For the flatpack, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch thick, epoxy-glass board with ten 0.03-inch-wide, 2 oz. copper conductors.

Electrical Characteristics at 25°C and V_{CC} = ± 15V (Unless Otherwise Specified)

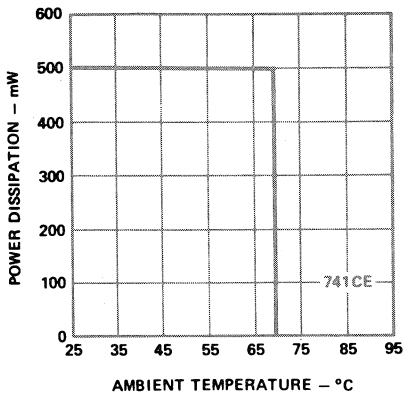
PARAMETER	CONDITIONS	741B			741C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			17	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance		0.3	2.0		0.3	2.0		MΩ
Input Capacitance			1.4			1.4		pF
Offset Voltage Adjustment Range			±50			±50		mV
Input Voltage Range		± 12	±13		± 12	±13		V
Large-Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{out} = ±10V	50	200		20	200		V/mV
Output Resistance			75			75		Ω
Output Short-Circuit Current			18			18		mA
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		30	150		30	150	μV/V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		70	90		dB
Supply Current			1.7	2.8		1.7	2.8	mA
Power Consumption			50	85		50	85	mW
Transient Response (unity gain)	V_{in} =20mV, R_L =2kΩ, $C_L \leq 100pF$							
Rise Time			0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew Rate	$R_L \geq 2k\Omega$	0.3	0.5		0.3	0.5		V/μs
The Following Specifications Apply Over the Operating Temperature Ranges:								
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input Offset Current	T_A max.		7.0	200		10	300	nA
	T_A min.		30	500		25	300	nA
Input Bias Current	T_A max.		0.03	0.5		0.04	0.8	μA
	T_A min.		0.3	1.5		0.13	0.8	μA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		30	150		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{out} = ±10V	25			15			V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		V
Supply Current	T_A max.		1.5	2.5		1.6	3.3	mA
	T_A min.		2.0	3.3		1.8	3.3	mA
Power Consumption	T_A max.		45	75		48	100	mW
	T_A min.		60	100		54	100	mW

Typical Characteristics

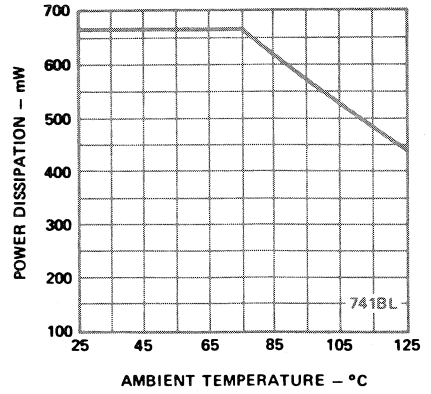
ABSOLUTE MAXIMUM POWER DISSIPATION



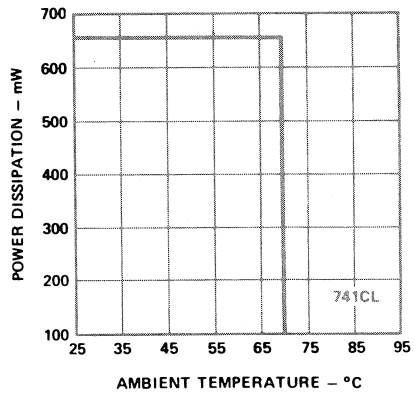
ABSOLUTE MAXIMUM POWER DISSIPATION



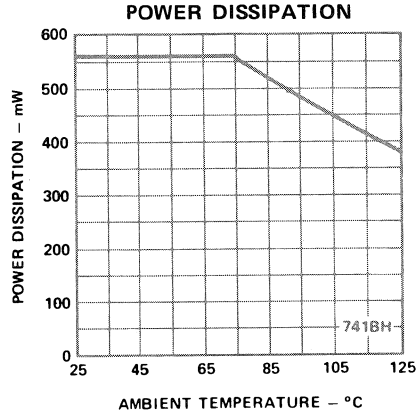
ABSOLUTE MAXIMUM POWER DISSIPATION



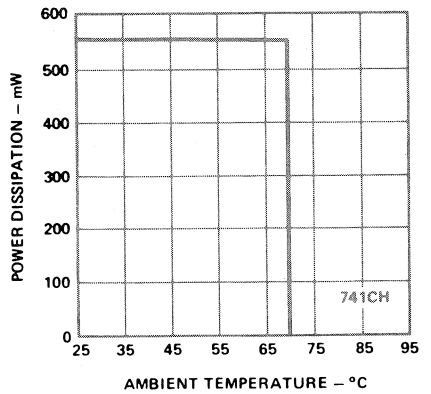
ABSOLUTE MAXIMUM POWER DISSIPATION



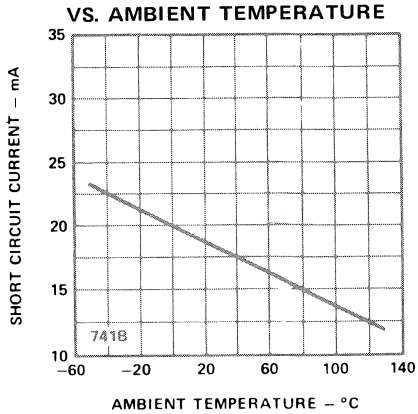
ABSOLUTE MAXIMUM POWER DISSIPATION



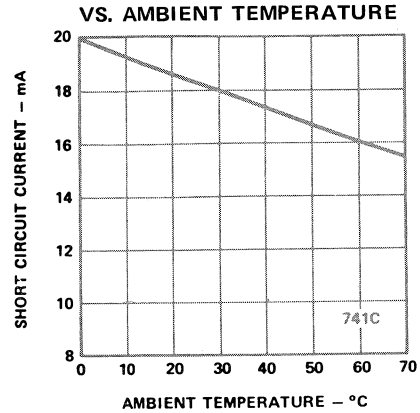
ABSOLUTE MAXIMUM POWER DISSIPATION



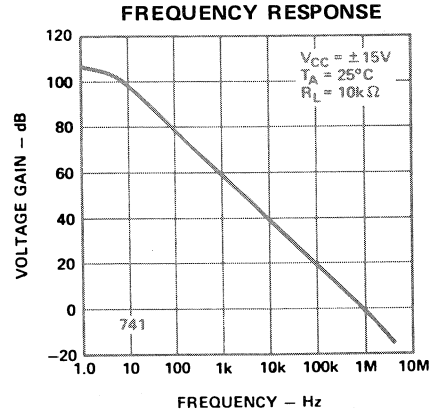
OUTPUT SHORT-CIRCUIT CURRENT VS. AMBIENT TEMPERATURE



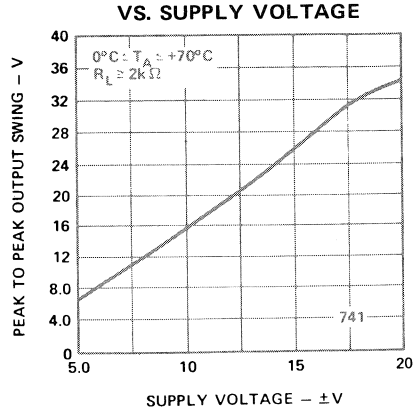
OUTPUT SHORT-CIRCUIT CURRENT VS. AMBIENT TEMPERATURE



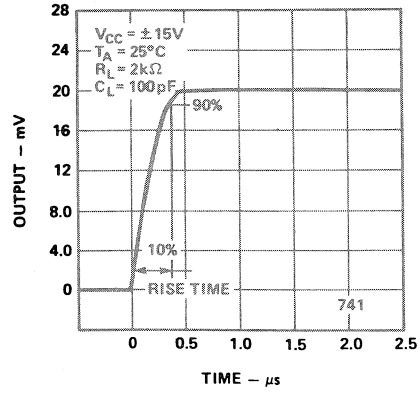
OPEN LOOP FREQUENCY RESPONSE



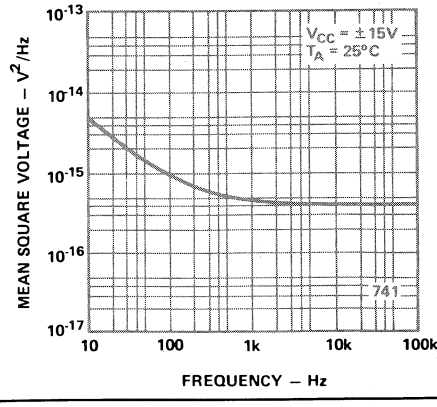
OUTPUT VOLTAGE SWING VS. SUPPLY VOLTAGE



TRANSIENT RESPONSE

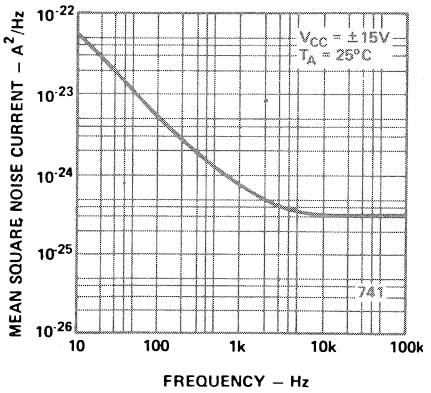


INPUT NOISE VOLTAGE VS. FREQUENCY

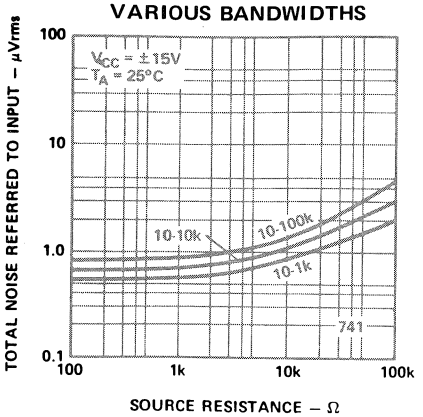


Typical Characteristics (Cont'd.)

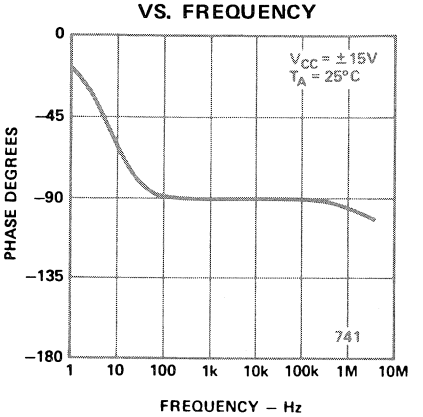
INPUT NOISE CURRENT VS. FREQUENCY



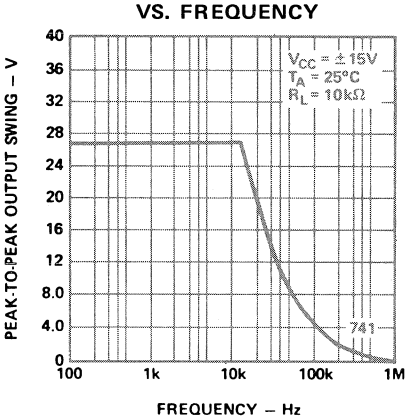
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



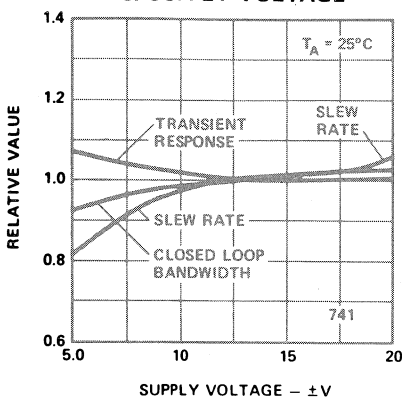
OPEN LOOP PHASE RESPONSE VS. FREQUENCY



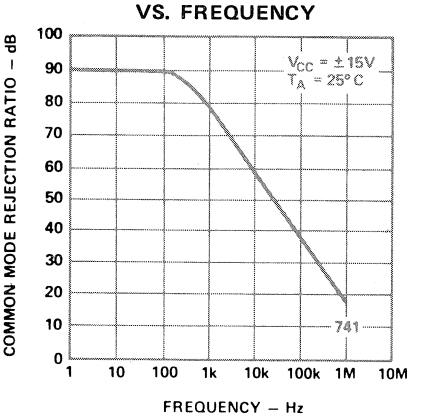
OUTPUT VOLTAGE SWING VS. FREQUENCY



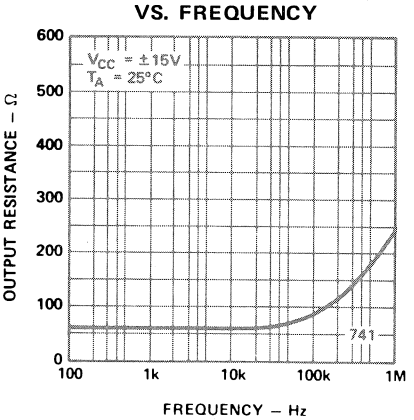
FREQUENCY CHARACTERISTICS VS. SUPPLY VOLTAGE



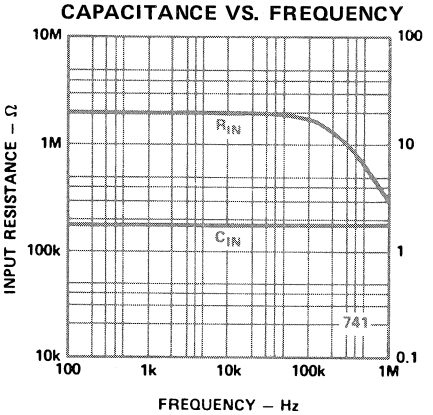
COMMON MODE REJECTION RATIO VS. FREQUENCY



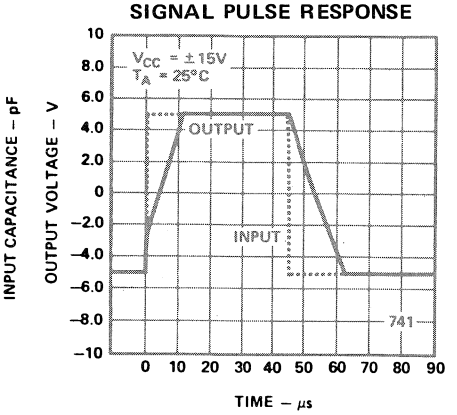
OUTPUT RESISTANCE VS. FREQUENCY



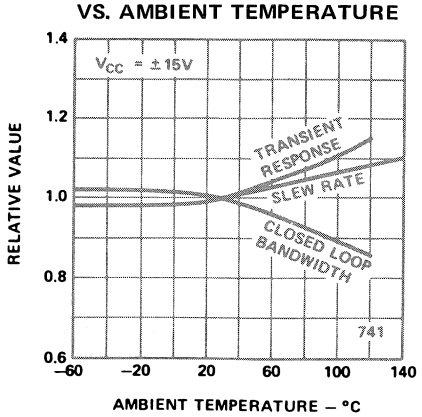
INPUT RESISTANCE AND INPUT CAPACITANCE VS. FREQUENCY



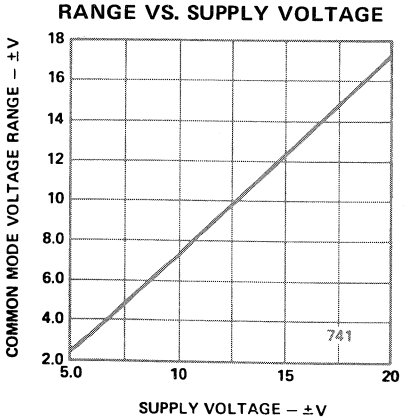
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



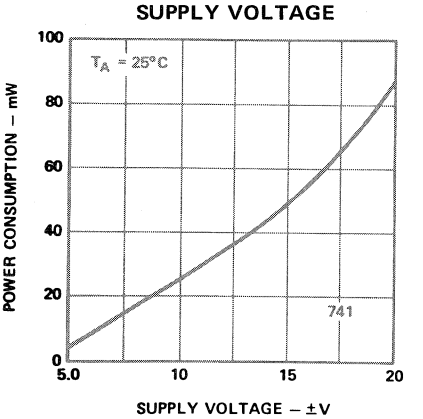
FREQUENCY CHARACTERISTICS VS. AMBIENT TEMPERATURE



INPUT COMMON MODE VOLTAGE RANGE VS. SUPPLY VOLTAGE

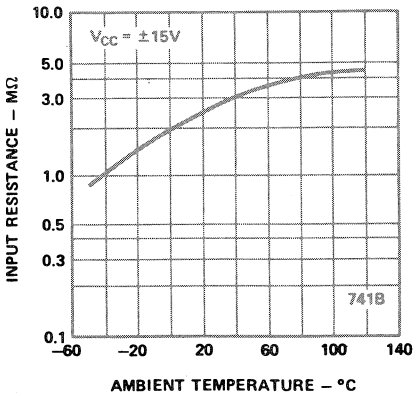


POWER CONSUMPTION VS. SUPPLY VOLTAGE

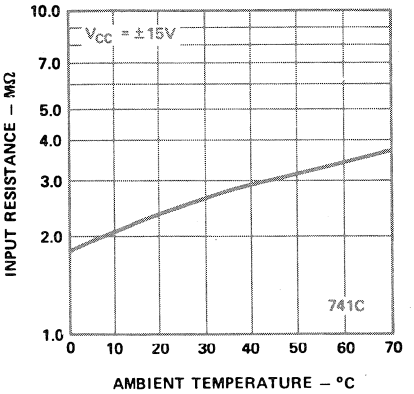


Typical Characteristics (Cont'd.)

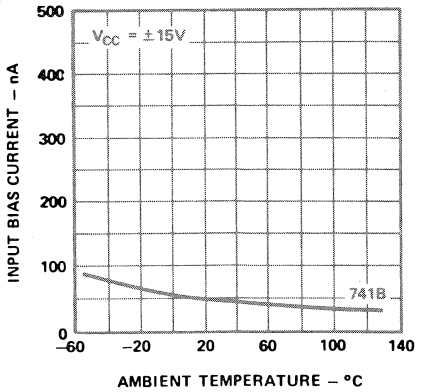
INPUT RESISTANCE VS. AMBIENT TEMPERATURE



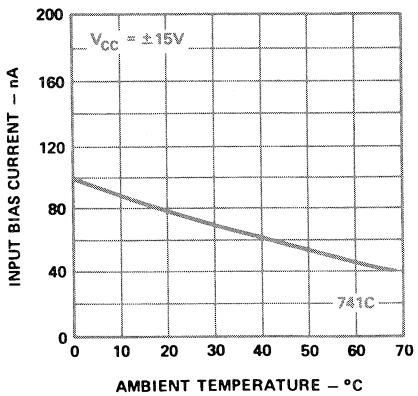
INPUT RESISTANCE VS. AMBIENT TEMPERATURE



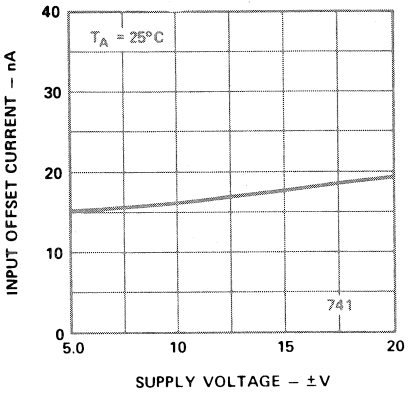
INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE



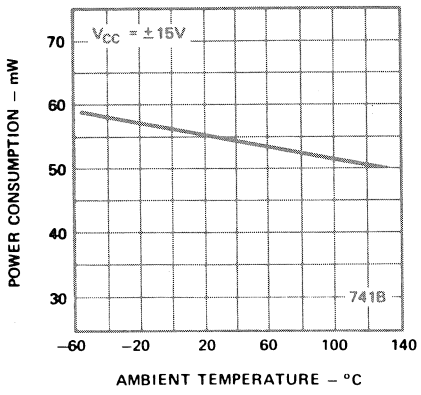
INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE



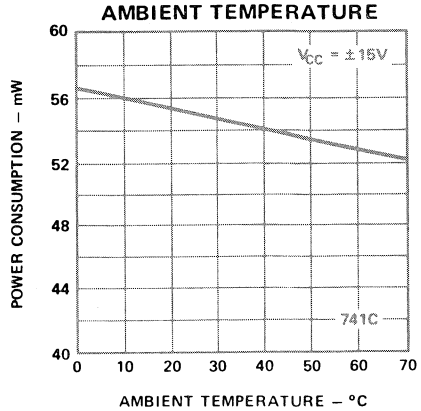
INPUT OFFSET CURRENT VS. SUPPLY VOLTAGE



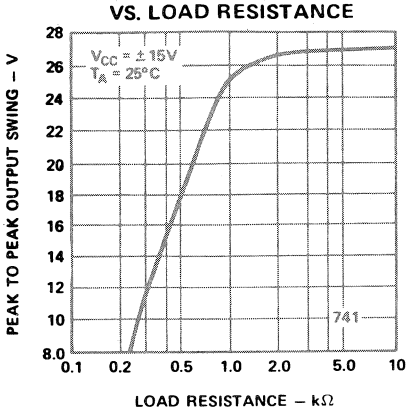
POWER CONSUMPTION VS. AMBIENT TEMPERATURE



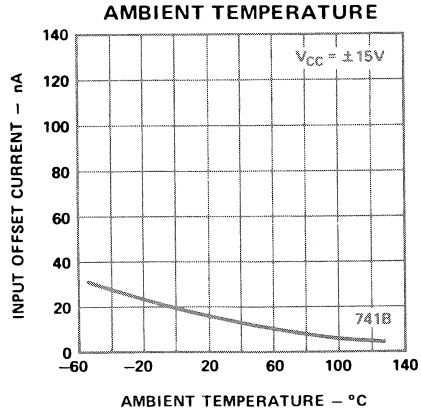
POWER CONSUMPTION VS. AMBIENT TEMPERATURE



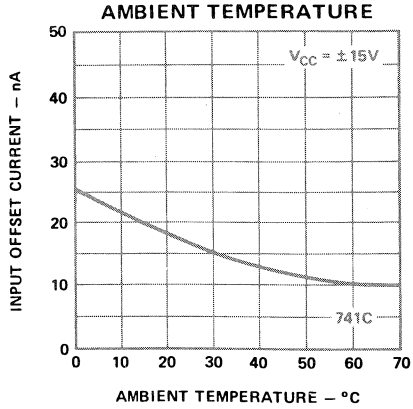
OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



INPUT OFFSET CURRENT VS. AMBIENT TEMPERATURE

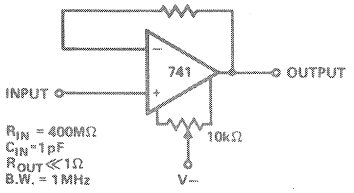


INPUT OFFSET CURRENT VS. AMBIENT TEMPERATURE

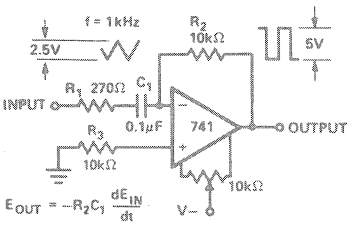


Typical Applications

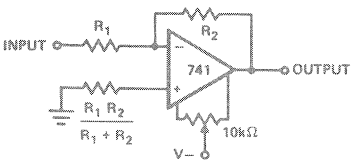
UNITY GAIN VOLTAGE FOLLOWER



DIFFERENTIATOR

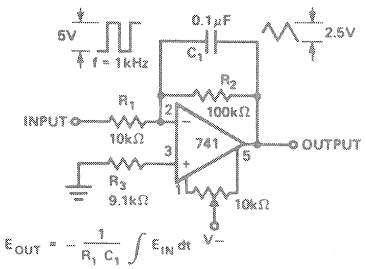


INVERTING AMPLIFIER

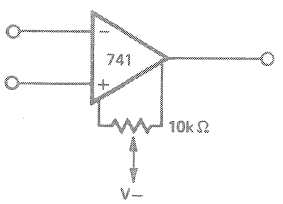


GAIN	R_1	R_2	B.W.	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

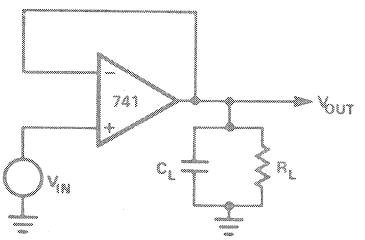
INTEGRATOR



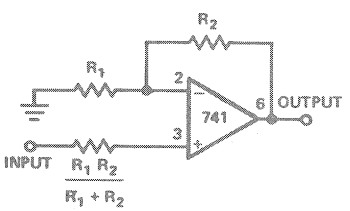
VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT

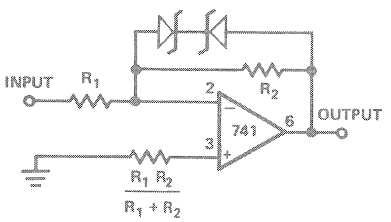


NON-INVERTING AMPLIFIER



GAIN	R_1	R_2	B.W.	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

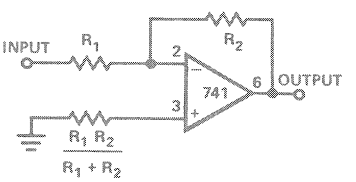
CLIPPING AMPLIFIER



$$\frac{E_{out}}{E_{IN}} = \frac{R_2}{R_1} \text{ if } |E_{out}| \ll V_Z + 0.7V$$

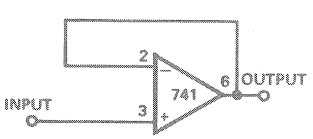
where V_Z = Zener breakdown voltage

INVERTING AMPLIFIER



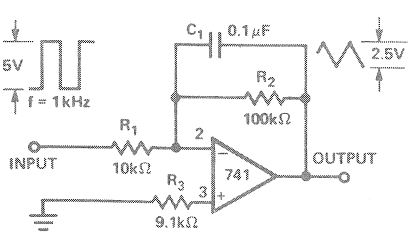
GAIN	R_1	R_2	B.W.	R_{IN}
1	10kΩ	10kΩ	1MHz	10kΩ
10	1kΩ	10kΩ	100kHz	1kΩ
100	1kΩ	100kΩ	10kHz	1kΩ
1000	100Ω	100kΩ	1kHz	100Ω

UNITY-GAIN VOLTAGE FOLLOWER



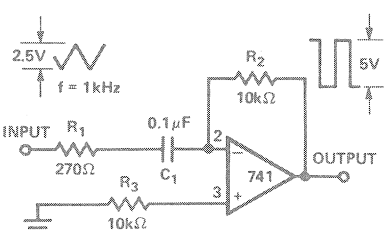
R_{IN} = 400MΩ
C_{IN} = 1pF
$R_{out} \ll 1\Omega$
B.W. = 1MHz

SIMPLE INTEGRATOR



$$E_{out} = -\frac{1}{R_1 C_1} \int E_{IN} dt$$

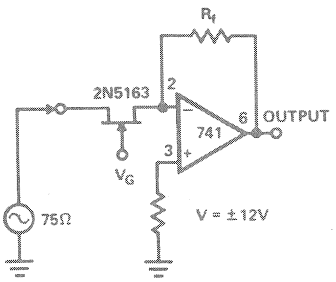
SIMPLE DIFFERENTIATOR

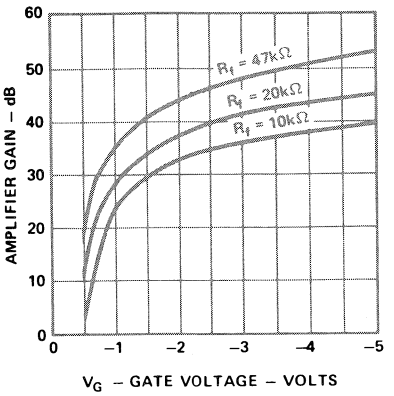


$$E_{out} = -R_2 C_1 \frac{dE_{IN}}{dt}$$

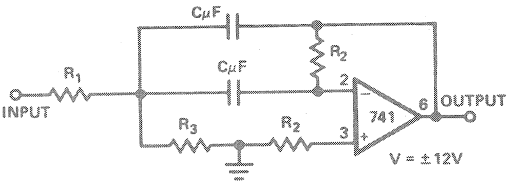
Typical Applications (Cont'd.)

GAIN CONTROLLED AMPLIFIER





BASIC ACTIVE FILTER



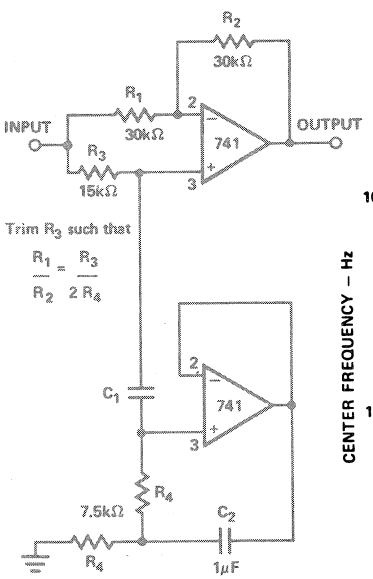
The values of the various components are given by:

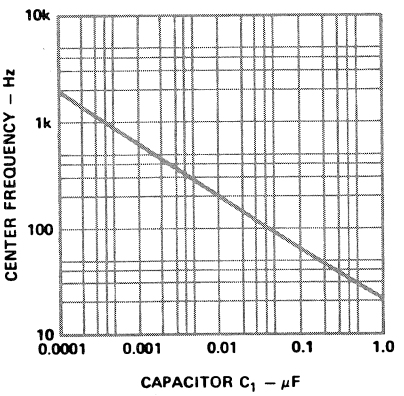
$$R_1 = \frac{1}{2\pi \Delta AC}$$

$$R_2 = \frac{1}{\Delta \pi C}$$

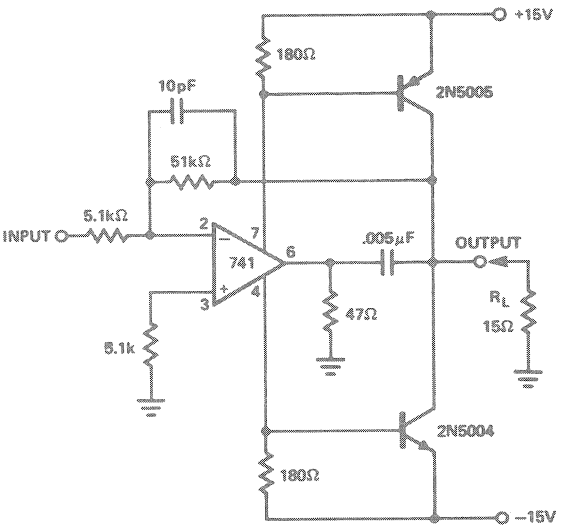
$$R_3 = \frac{1}{2\pi C\left[\frac{2f_o^2}{\Delta} - \Delta A\right]}$$

NOTCH FILTER USING THE μA 741 AS A GYRATOR





HIGH SLEW RATE POWER AMPLIFIER



747
Dual Operational Amplifiers

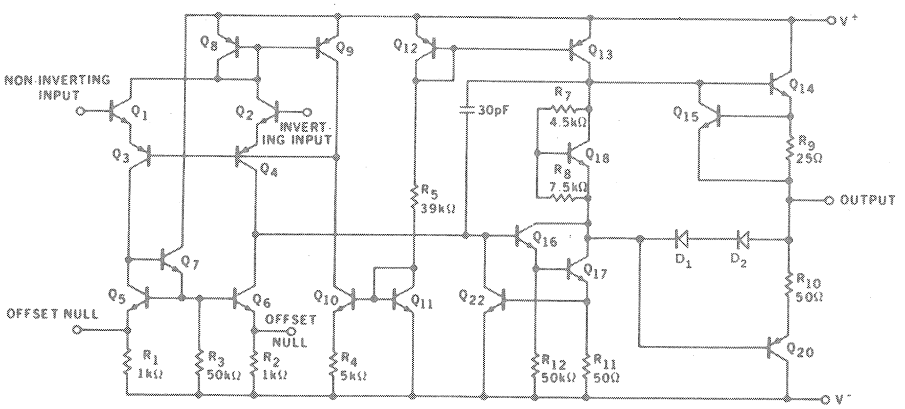
Features

- INTERNAL COMPENSATION ELIMINATES EXTERNAL COMPENSATION COMPONENTS
- OUTPUT SHORT CIRCUIT PROTECTION
- OFFSET NULL CAPABILITY
- LOW POWER CONSUMPTION
- LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES

Description

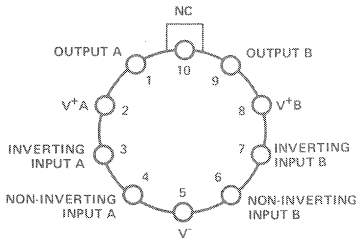
The Teledyne 747 is a dual 741 general purpose operational amplifier constructed on a monolithic chip using the planar epitaxial process. Frequency compensation is provided internally on the chip, and the 6dB/octave roll-off insures stability in closed-loop applications. It is internally short-circuit protected and requires no external components for frequency compensation which makes it ideal wherever board space and weight are important. High common mode voltage range and freedom from "latch-up" characteristics make the device useful in voltage follower applications. Its high gain and wide range of operating voltage provide superior performance in integrator, summing amplifier and general feedback applications.

Equivalent Circuit Diagram



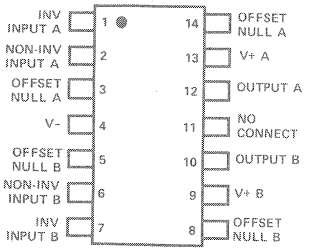
Connection Diagrams

E PACKAGE
10 LEAD METAL CAN
(TOP VIEW)



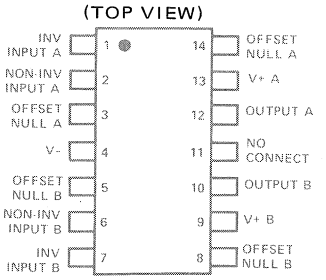
Order Part Numbers:
747BE (−55°C/+125°C)
747CE (0°C/+70°C)

J PACKAGE
14 LEAD PLASTIC DIP
(TOP VIEW)



Order Part Number:
747CJ (0°C/+70°C)

N PACKAGE
14 LEAD CERDIP
(TOP VIEW)



Order Part Number:
747BN (−55°C/+125°C)

Absolute Maximum Ratings

	747B	747C
Differential Input Voltage	±22V	±18V
Input Voltage (Note 1)	±15V	±15V
Output Short Circuit Duration (Note 2)	Indefinite	Indefinite
Supply Voltage	±22V	±18V
Voltage Between Offset Null and V^-	±0.5V	±0.5V
Internal Power Dissipation (Note 3)		
Metal Can (E)	500mW	500mW
Ceramic Dual-In-Line (N)	670mW	670mW
Plastic Dual-In-Line (J)	NA	530mW
Storage Temperature Range	−65°C/+150°C	−65°C/+150°C
Operating Temperature Range	−55°C/+125°C	0°C/+70°C
Lead Soldering Temperature (60 sec.)	300°C	300°C
Junction Temperature	150°C	150°C

The above ratings are not meant to imply operation at each of these extremes simultaneously. Exceeding any or all of the absolute maximum ratings may cause permanent damage to the device.

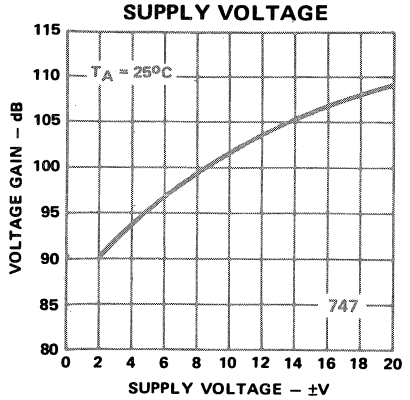
NOTES: 1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies to ambient temperatures up to 75°C ambient. For operation above T_A = 75°C, derate linearly 6.7mW/°C for the metal can, 8.9mW/°C for the ceramic dual-in-line.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

Electrical Characteristics

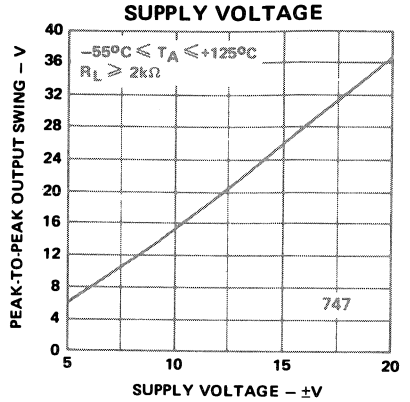
PARAMETER	CONDITIONS	747B			747C			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	$R_S \leq 10K\Omega$		1.0	5.0		1.0	6.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance		0.3	2.0		0.3	2.0		MΩ
Input Capacitance			1.4			1.4		pF
Offset Voltage Adjustment Range			±15			±15		mV
Large Signal Voltage Gain	$R_L \geq 2K\Omega$, V_{OUT} = ±10V	50,000	200K		25,000	200K		V/V
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Current			1.7	2.8		1.7	2.8	mA
Power Consumption			50	85		50	85	mW
Transient Response Risetime	V_{IN} = 20mV, R_L = 2KΩ,		0.3			0.3		μs
(Unity Gain) Overshoot	$C_L \leq 100pF$		5.0			5.0		%
Slew Rate	$R_L \geq 2K\Omega$		0.5			0.5		V/μs
Channel Separation			120			120		dB
The Following Specifications Apply Over the Operating Temperature Ranges:								
Input Offset Voltage	$R_S \leq 10K\Omega$		1.0	6.0		1.0	7.5	mV
Input Offset Current	T_A max. T_A min.		7.0 85	200 500		7.0	300	nA
Input Bias Current	T_A max. T_A min.		0.03 0.3	0.5 1.5		0.03	0.8	μA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10K\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10K\Omega$		30	150		30	150	μV/V
Large Signal Voltage Gain	$R_L \geq 2K\Omega$, V_{OUT} = ±10V	25,000			15,000			V/V
Output Voltage Swing	$R_L \geq 10K\Omega$ $R_L \geq 2K\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Supply Current	T_A max. T_A min.		1.5 2.0	2.5 3.3		2.0	3.3	mA
Power Consumption	T_A max. T_A min.		45 60	75 100		60	100	mW

Typical Characteristics

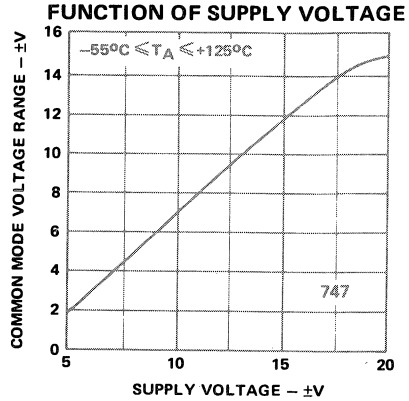
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



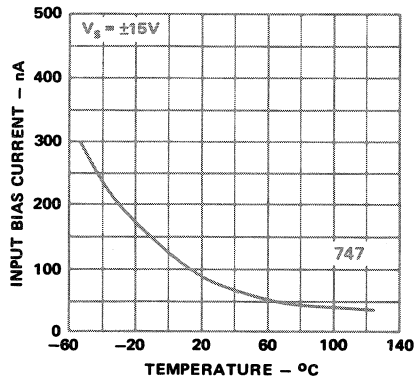
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



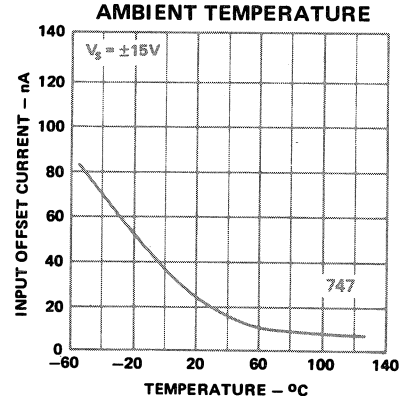
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



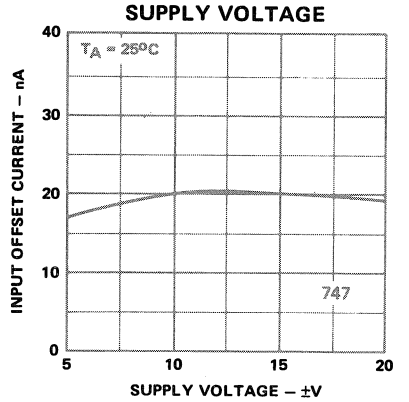
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



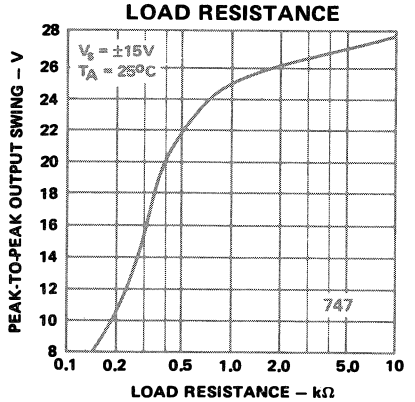
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



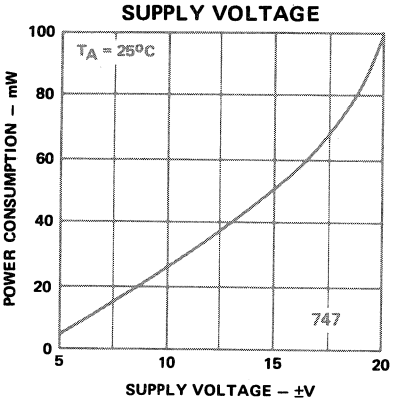
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



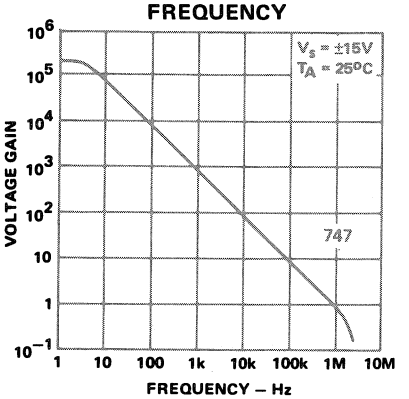
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



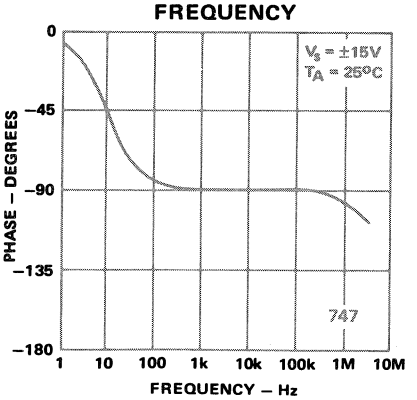
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



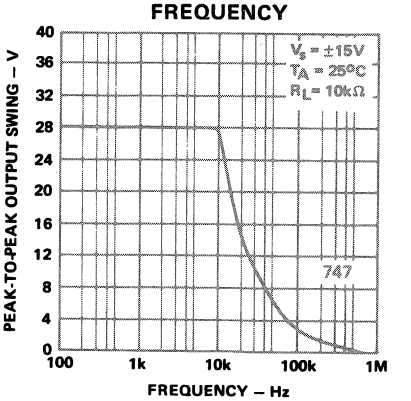
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



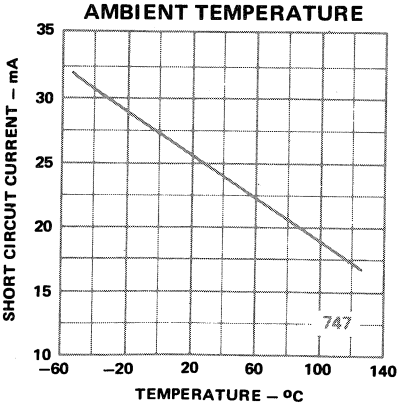
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

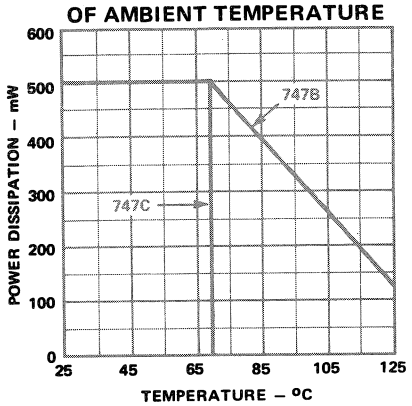


OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

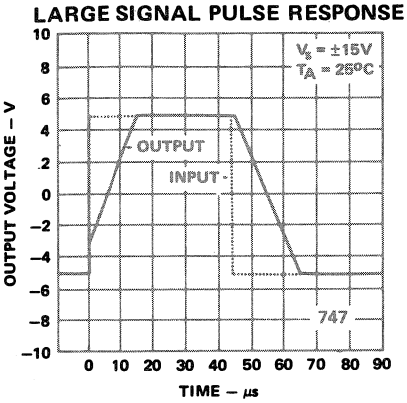


Typical Characteristics (Cont'd.)

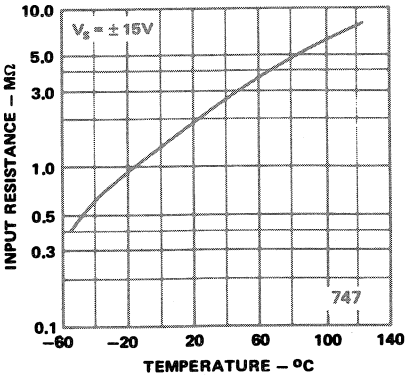
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



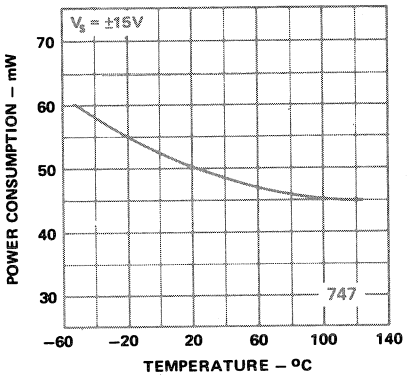
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



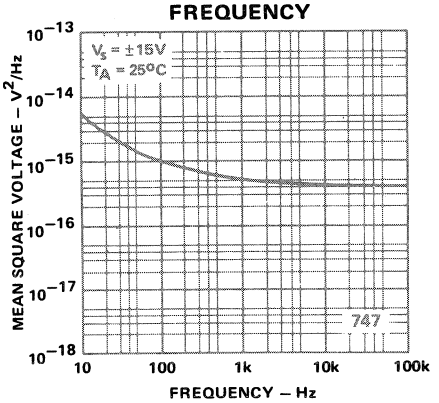
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



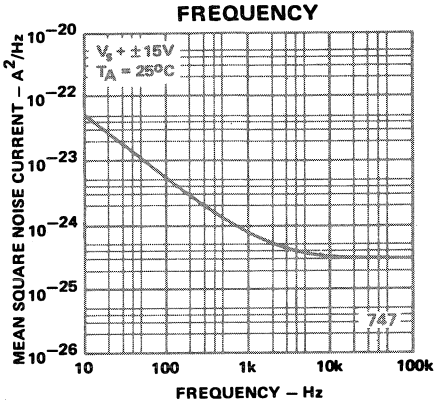
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



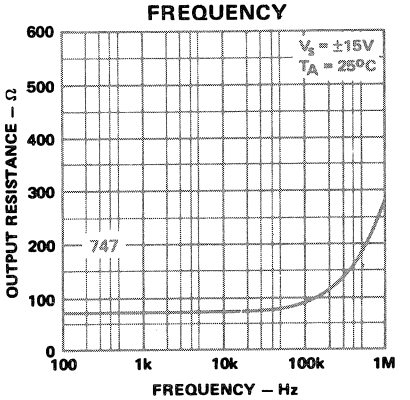
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



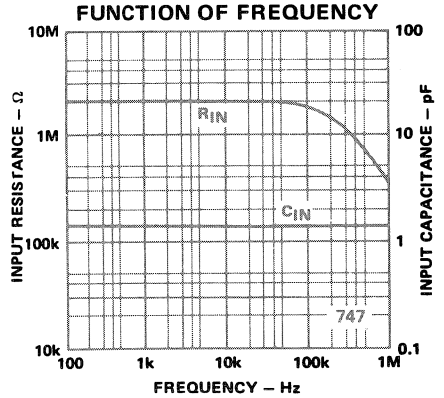
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



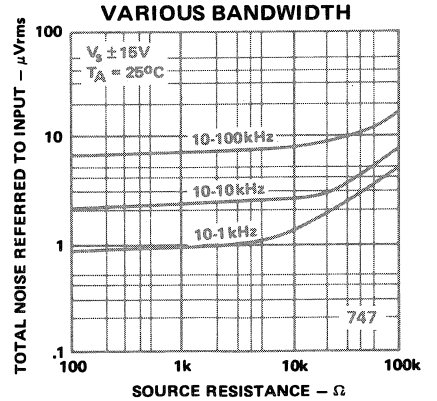
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



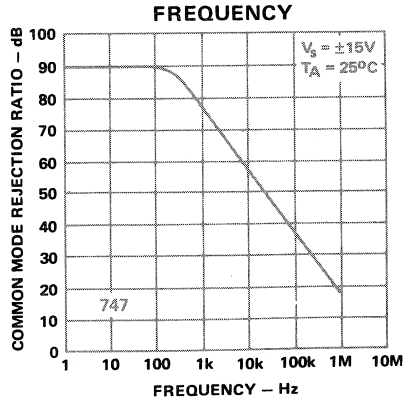
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



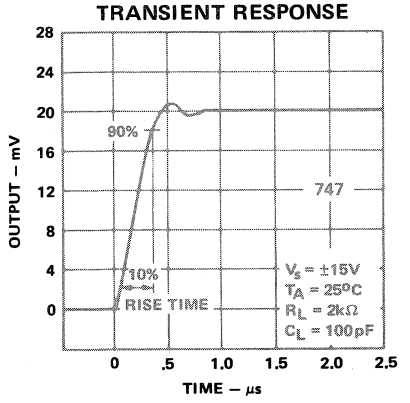
BROADBAND NOISE FOR VARIOUS BANDWIDTH



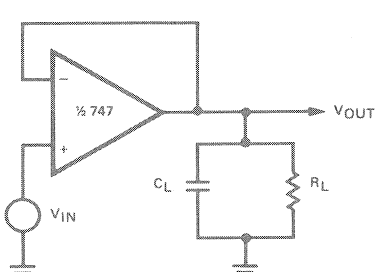
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



TRANSIENT RESPONSE

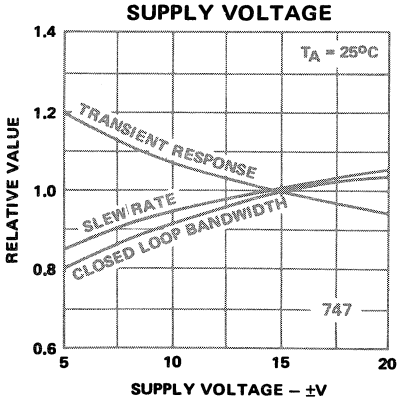


TRANSIENT RESPONSE TEST CIRCUIT

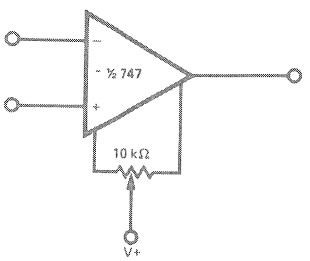


Typical Characteristics (Cont'd.)

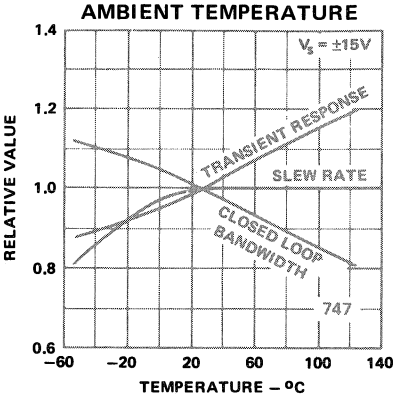
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE OFFSET NULL CIRCUIT

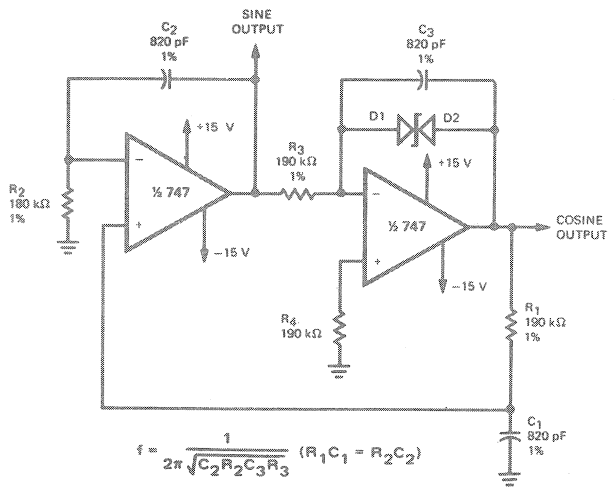


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

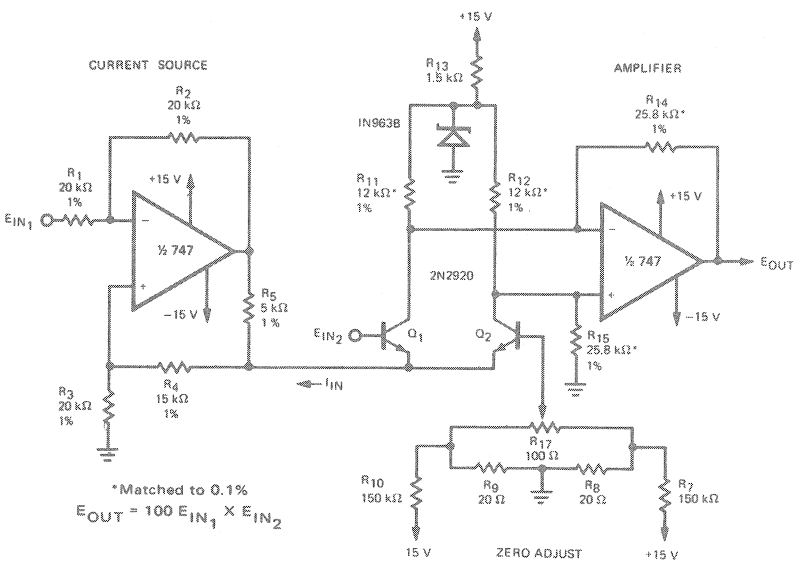


Typical Applications

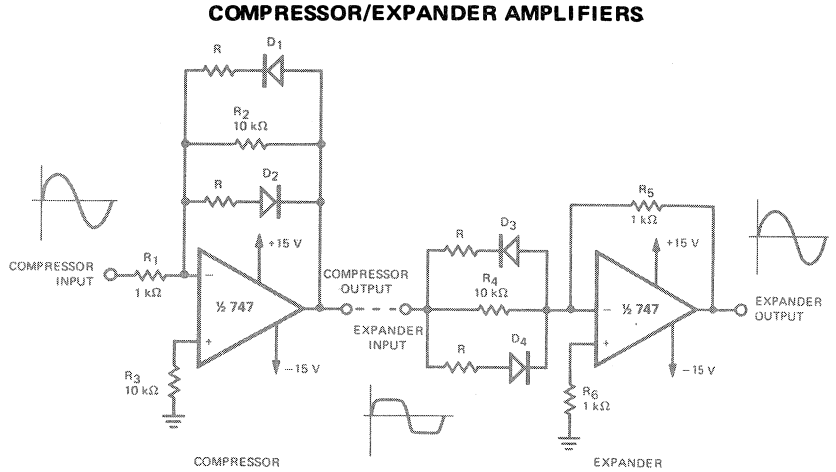
QUADRATURE OSCILLATOR



ANALOG MULTIPLIER

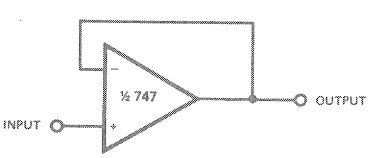


COMPRESSOR/EXPANDER AMPLIFIERS



MAXIMUM COMPRESSION EXPANSION RATIO = R_1/R (10 kΩ > R ≥0)
NOTE: DIODES D_1 THROUGH D_4 ARE MATCHED FD6666 OR EQUIVALENT

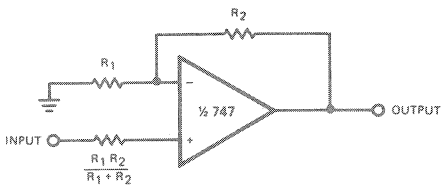
UNITY-GAIN VOLTAGE FOLLOWER



R_{IN} = 400 MΩ
C_{IN} = 1 pF
$R_{OUT} << 1\ \Omega$
B W = 1 MHz

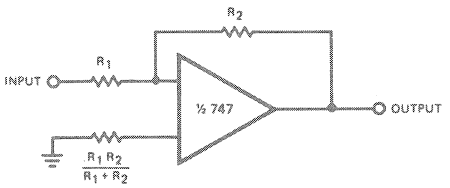
Typical Applications (Cont'd.)

NON-INVERTING AMPLIFIER



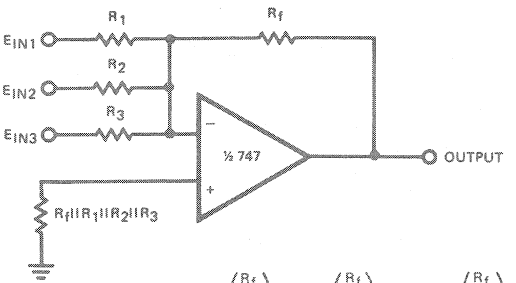
GAIN	R_1	R_2	B.W.	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

INVERTING AMPLIFIER



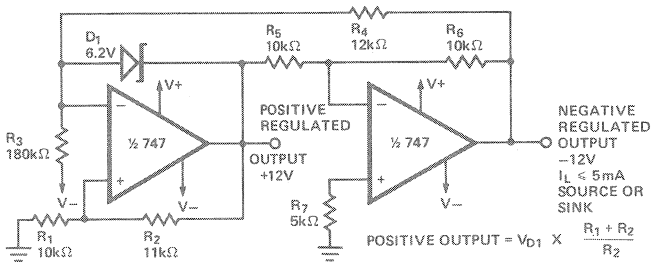
GAIN	R_1	R_2	B W	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

WEIGHTED AVERAGING AMPLIFIER



$$-E_{OUT} = E_{IN1}\left(\frac{R_f}{R_1}\right) + E_{IN2}\left(\frac{R_f}{R_2}\right) + E_{IN3}\left(\frac{R_f}{R_3}\right)$$

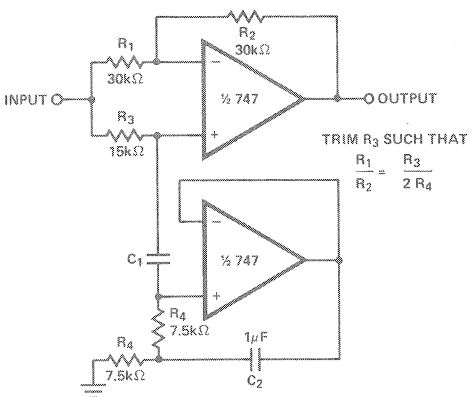
TRACKING POSITIVE AND NEGATIVE VOLTAGE REFERENCES

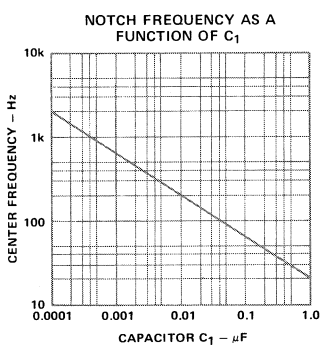


$$\text{POSITIVE OUTPUT} = V_{D1} \times \frac{R_1 + R_2}{R_2}$$

$$\text{NEGATIVE OUTPUT} = -\text{POSITIVE OUTPUT} \times \frac{R_6}{R_5}$$

NOTCH FILTER USING THE 747 AS A GYRATOR





748
Operational Amplifiers

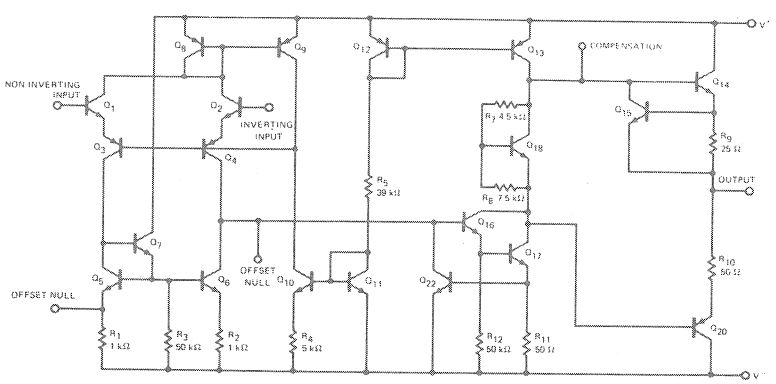
Features

- SHORT-CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH UP

Description

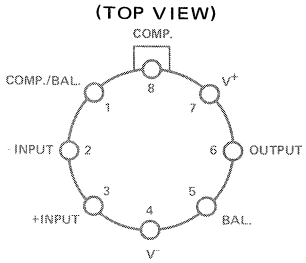
The Teledyne 748 is a high performance monolithic operational amplifier constructed using the planar epitaxial process. It is intended for a high wide range of analog applications where tailoring of frequency characteristics is desirable. High common mode voltage range and absence of "latch-up" make the 748 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The 748 is short-circuit protected and has the same pin configuration as the popular 741 operational amplifier. Unity gain frequency compensation is achieved by means of a single 30pF capacitor. The 748B is intended for operation from −55°C to +125°C. The 748C commercial version operates from 0°C to +70°C.

Equivalent Circuit Diagram



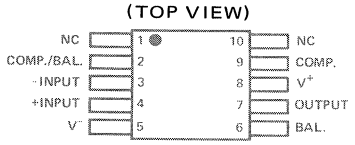
Connection Diagrams

E PACKAGE
8 LEAD METAL CAN
(TOP VIEW)



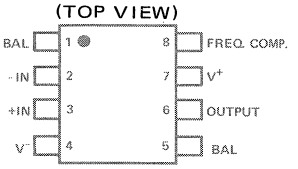
Order Part Numbers:
748BE, 748CE

H PACKAGE
10 LEAD FLATPACK
(TOP VIEW)



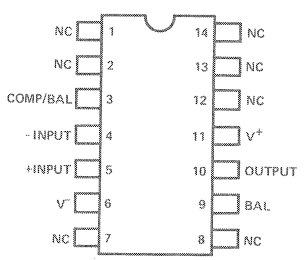
Order Part Number:
748BH

P PACKAGE
8 LEAD MINIDIP
(TOP VIEW)



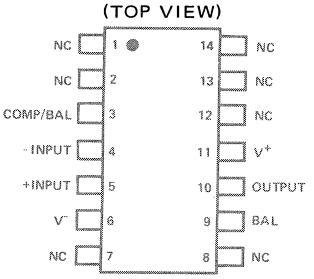
Order Part Number:
748CP

L PACKAGE
14 LEAD CERDIP
(TOP VIEW)



Order Part Numbers:
748BL, 748CL

J PACKAGE
14 LEAD PLASTIC DIP
(TOP VIEW)



Order Part Number:
748CJ

Absolute Maximum Ratings

Input Voltage (Note 1)	±15V
Differential Input Voltage	±30V
Output Short Circuit Duration (Note 2)	Indefinite
Supply Voltage	±22V
Internal Power Dissipation (Note 3)	
Metal Can	500mW
DIP	670mW
Mini DIP	310mW
Flatpak	570mW
Storage Temperature Range	
Metal Can	−65°C to +150°C
Mini DIP	−55°C to +125°C
Operating Temperature Range	
Military (748)	−55°C to +125°C
Commercial (748C)	0°C to +70°C
Lead Temperature (Soldering, 60 Seconds)	
Metal Can	300°C
Mini DIP	260°C

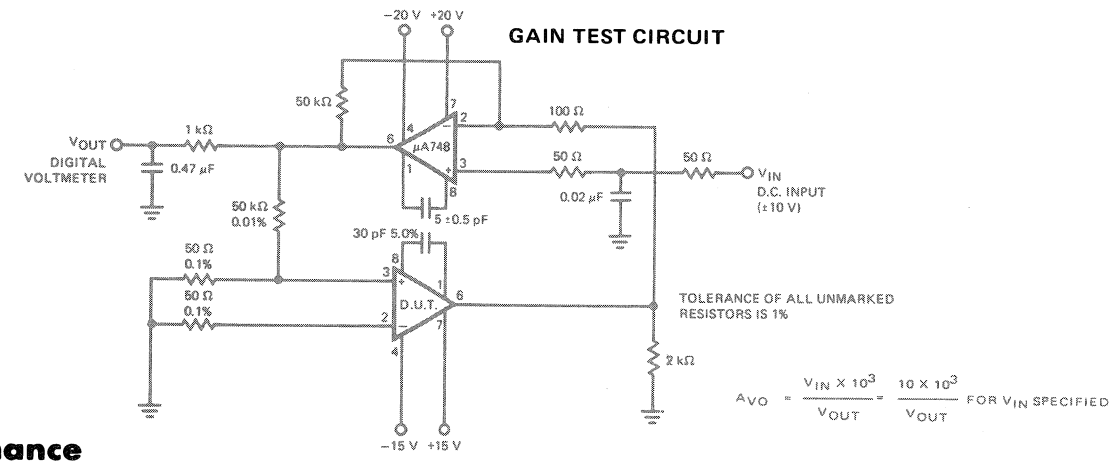
Electrical Characteristics (V_S = ±15V, T_A = 25°C, C_C = 30pF unless otherwise specified)

PARAMETER	CONDITIONS	748B			748C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10K\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance		0.3	2.0		0.3	2.0		MΩ
Input Capacitance			2.0			2.0		pF
Offset Voltage Adjustment Range			±15			±15		mV
Large Signal Voltage Gain	$R_L \geq 2K\Omega$, V_{OUT} = ±10V	50,000	150,000		20,000	150,000		V/V
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Current			1.9	2.8		1.9	2.8	mA
Power Consumption			60	85		60	85	mW
Transient Response (Voltage Follower, Gain of 1) — Risetime	V_{IN} = 20mV, C_C = 30pF, R_L = 2KΩ, $C_L \leq$ 100pF		0.3			0.3		μs
Transient Response (Voltage Follower, Gain of 1) — Overshoot	V_{IN} = 20mV, C_C = 30pF, R_L = 2KΩ, $C_L \leq$ 100pF		5.0			5.0		%
Slew Rate (Voltage Follower, Gain of 1)	$R_L \geq 2K\Omega$		0.5			0.5		V/μs
Transient Response (Voltage Follower, Gain of 1) — Risetime	V_{IN} = 20mV, C_C = 3.5pF, R_L = 2KΩ, $C_L \leq$ 100pF		0.2			0.2		μs
Transient Response (Voltage Follower, Gain of 1) — Overshoot	V_{IN} = 20mV, C_C = 3.5pF, R_L = 2KΩ, $C_L \leq$ 100pF		5.0			5.0		%
Slew Rate (Voltage Follower, Gain of 10)	$R_L \geq 2K\Omega$, C_C = 3.5pF		5.5			5.5		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$:								
Input Offset Voltage	$R_S \leq 10K\Omega$		1.0	6.0			7.5	mV
Input Offset Current	T_A = +125°C		10	200				nA
Input Offset Current	T_A = −55°C		50	500				nA
Input Offset Current							300	nA
Input Bias Current	T_A = +125°C		0.03	0.5				μA
Input Bias Current	T_A = −55°C		0.3	1.5				μA
Input Bias Current							800	nA

Electrical Characteristics (Cont'd.)

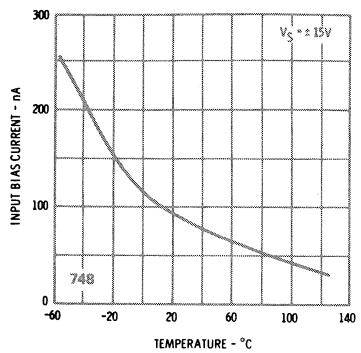
PARAMETER	CONDITIONS	748B MIN	748B TYP	748B MAX	748C MIN	748C TYP	748C MAX	UNITS
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10K\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10K\Omega$		30	150		30	150	μV/V
Large Signal Voltage Gain	$R_L \geq 2K\Omega$, $V_{OUT} = \pm 10V$	25,000			15,000			V/V
Output Voltage Swing	$R_L \geq 10K\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2K\Omega$	±10	±13		±10	±13		V
Supply Current	$T_A = +125°C$		1.5	2.5				mA
	$T_A = -55°C$		2.0	3.3				mA
Power Consumption	$T_A = +125°C$		45	75				mW
	$T_A = -55°C$		60	100				mW
Power Consumption						60	100	mW

Test Circuits

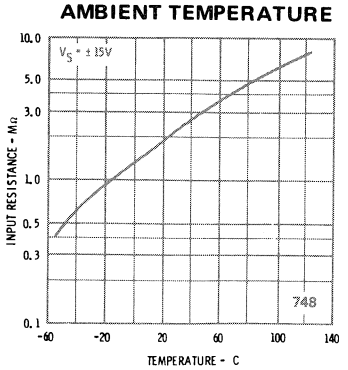


Typical Performance

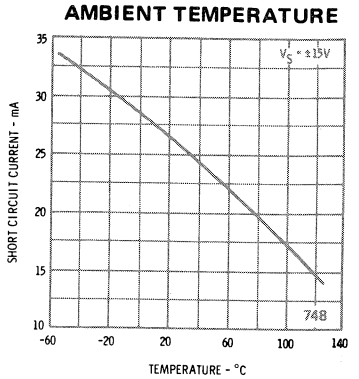
INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE



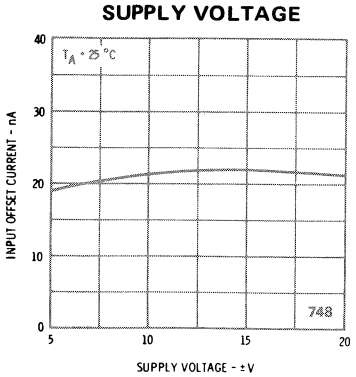
INPUT RESISTANCE VS. AMBIENT TEMPERATURE



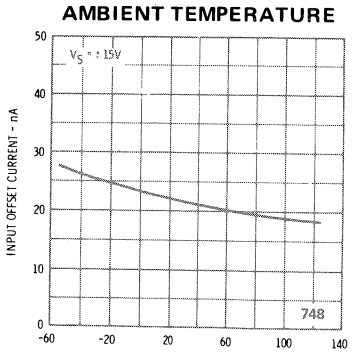
OUTPUT SHORT-CIRCUIT CURRENT VS. AMBIENT TEMPERATURE



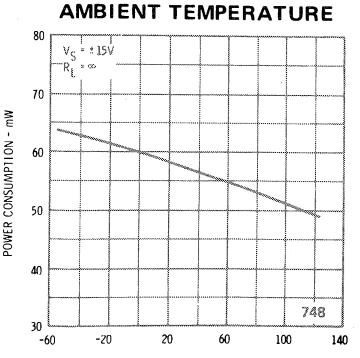
INPUT OFFSET CURRENT VS. SUPPLY VOLTAGE



INPUT OFFSET CURRENT VS. AMBIENT TEMPERATURE

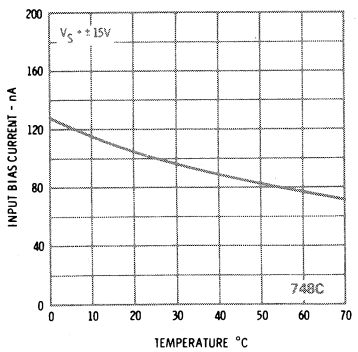


POWER CONSUMPTION VS. AMBIENT TEMPERATURE

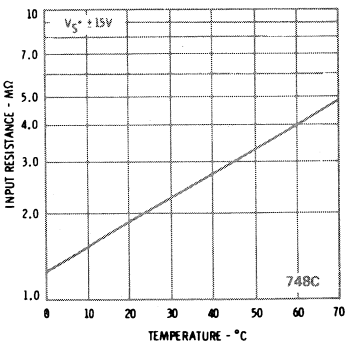


Typical Performance

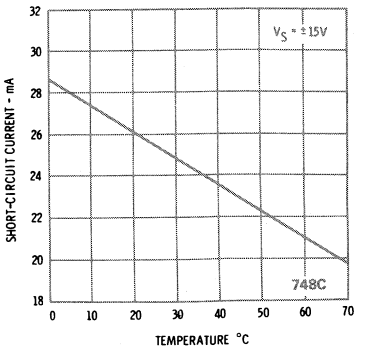
INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE



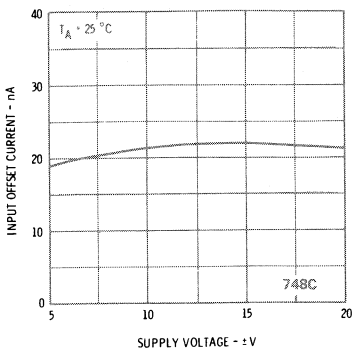
INPUT RESISTANCE VS. AMBIENT TEMPERATURE



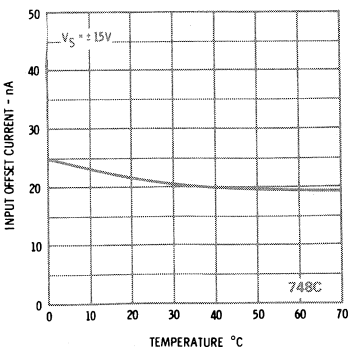
OUTPUT SHORT-CIRCUIT CURRENT VS. AMBIENT TEMPERATURE



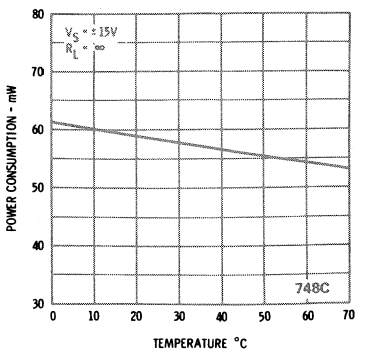
INPUT OFFSET CURRENT VS. SUPPLY VOLTAGE



INPUT OFFSET CURRENT VS. AMBIENT TEMPERATURE

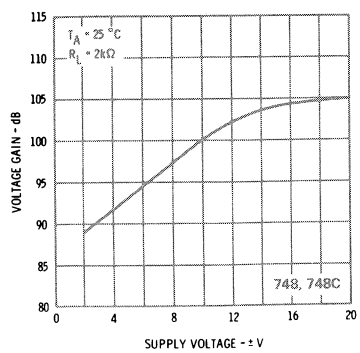


POWER CONSUMPTION VS. AMBIENT TEMPERATURE

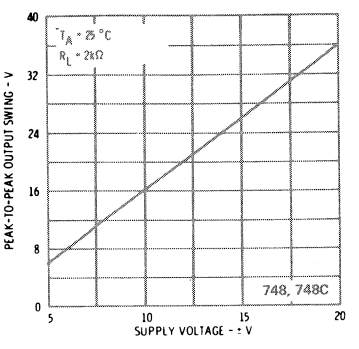


TYPICAL PERFORMANCE CURVES FOR 748 AND 748C

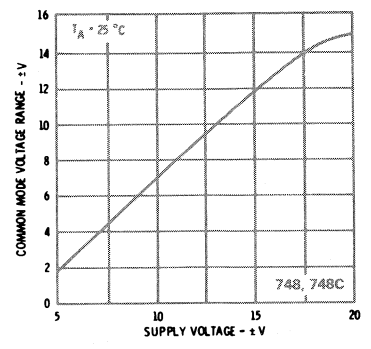
OPEN LOOP VOLTAGE GAIN VS. SUPPLY VOLTAGE



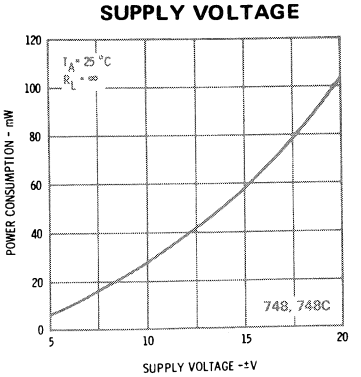
OUTPUT VOLTAGE SWING VS. SUPPLY VOLTAGE



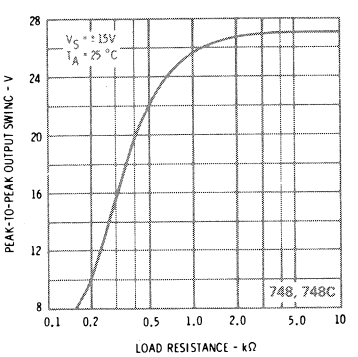
INPUT COMMON MODE VOLTAGE RANGE VS. SUPPLY VOLTAGE



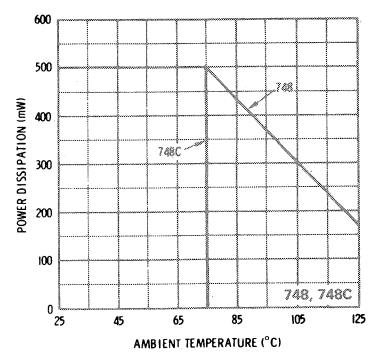
POWER CONSUMPTION VS. SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



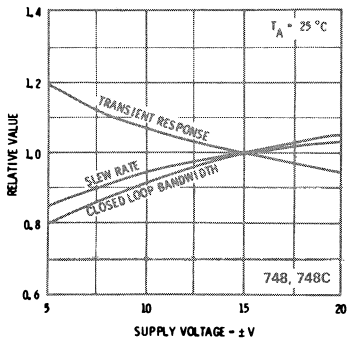
ABSOLUTE MAXIMUM POWER DISSIPATION VS. AMBIENT TEMPERATURE



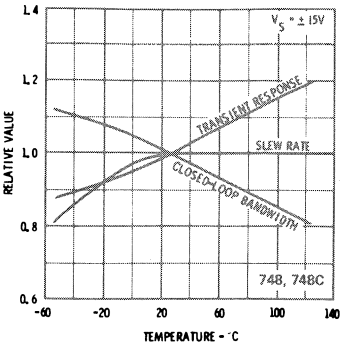
Typical Performance

TYPICAL PERFORMANCE CURVES FOR 748 AND 748C

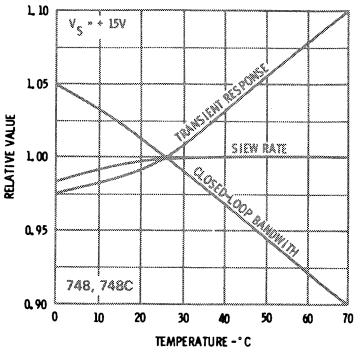
FREQUENCY CHARACTERISTICS VS. SUPPLY VOLTAGE



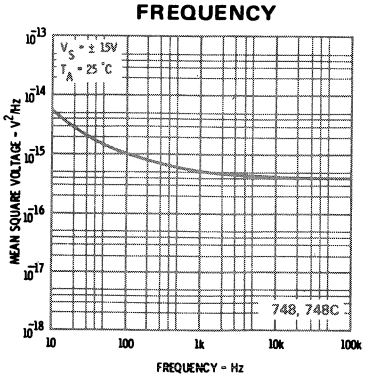
748 FREQUENCY CHARACTERISTICS VS. AMBIENT TEMPERATURE



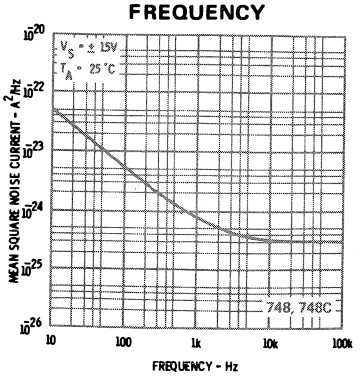
748C FREQUENCY CHARACTERISTICS VS. AMBIENT TEMPERATURE



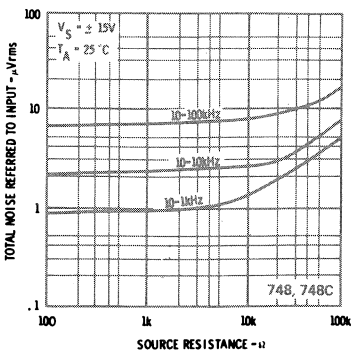
INPUT NOISE VOLTAGE VS. FREQUENCY



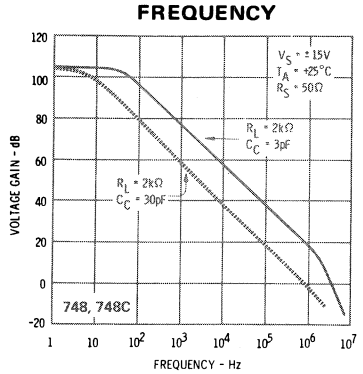
INPUT NOISE CURRENT VS. FREQUENCY



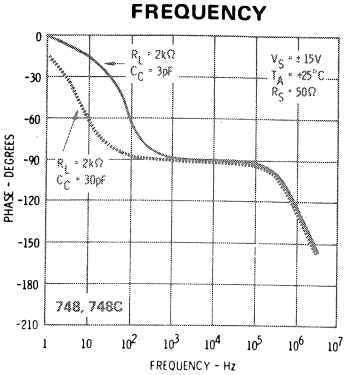
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



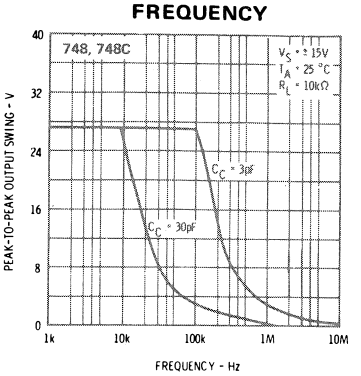
OPEN LOOP VOLTAGE GAIN VS. FREQUENCY



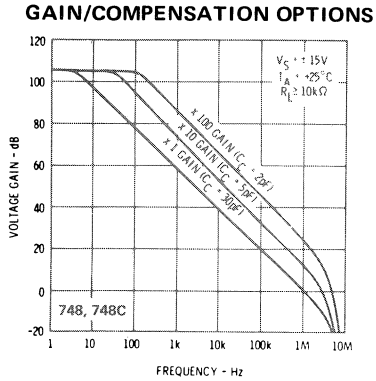
OPEN LOOP PHASE RESPONSE VS. FREQUENCY



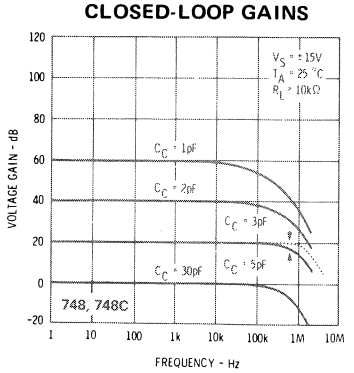
OUTPUT VOLTAGE SWING VS. FREQUENCY



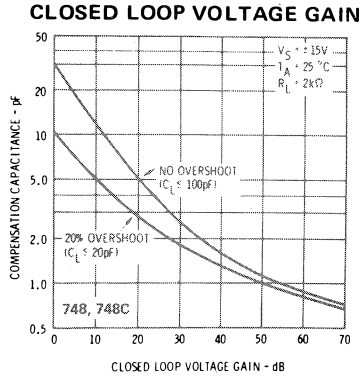
OPEN LOOP VOLTAGE GAIN VS. FREQUENCY FOR VARIOUS GAIN/COMPENSATION OPTIONS



FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS

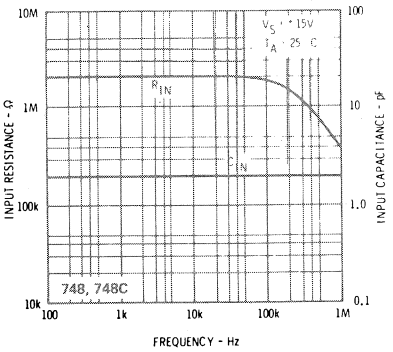


COMPENSATION CAPACITANCE VS. CLOSED LOOP VOLTAGE GAIN

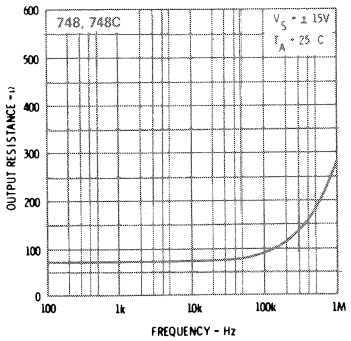


Typical Performance

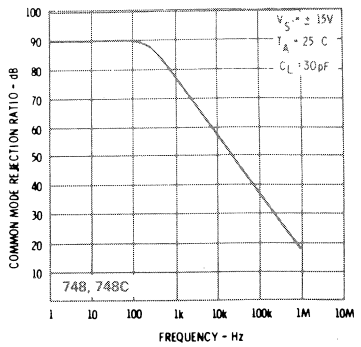
INPUT RESISTANCE AND INPUT CAPACITANCE VS. FREQUENCY



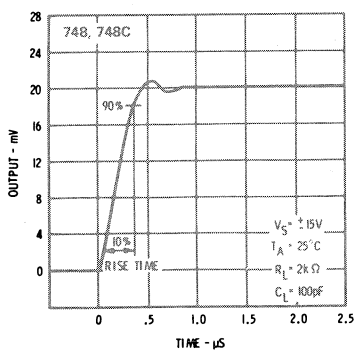
OUTPUT RESISTANCE VS. FREQUENCY



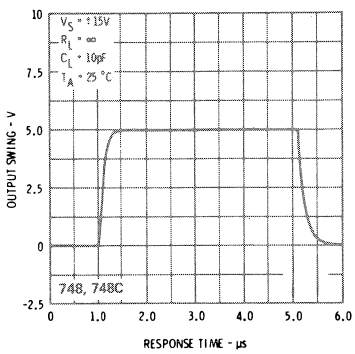
COMMON MODE REJECTION RATIO VS. FREQUENCY



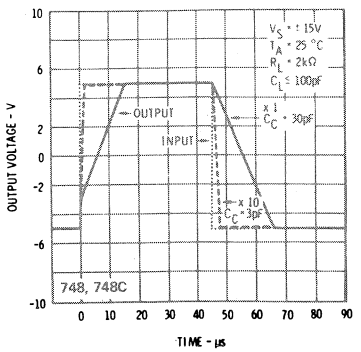
VOLTAGE FOLLOWER TRANSIENT RESPONSE (GAIN OF 1)



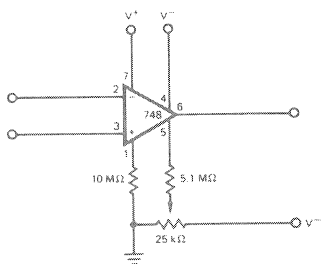
LARGE SIGNAL FEED–FORWARD TRANSIENT RESPONSE



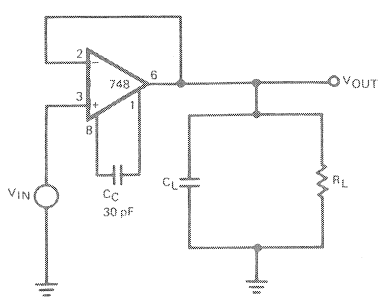
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



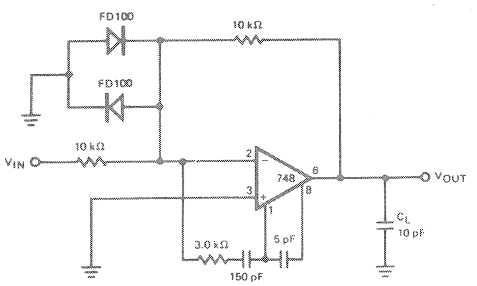
VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



FEED-FORWARD COMPENSATION



835*
Quad 741-Type Operational Amplifiers

Features

- LOW CROSSOVER DISTORTION
- INPUT COMMON MODE RANGE INCLUDES THE NEGATIVE SUPPLY
- REPLACES THE LM124/224/324 IN SPLIT SUPPLY APPLICATIONS (±1.5V TO ±18V)
- INTERNAL FREQUENCY COMPENSATION
- LOW IMPEDANCE SHORT CIRCUIT PROTECTED OUTPUTS
- LOW AMPLIFIER POWER CONSUMPTION

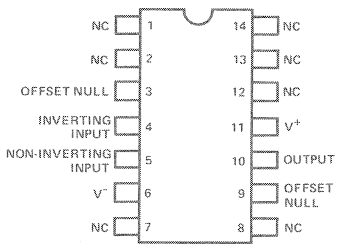
Description

The 835 is a monolithic integrated circuit containing four internally compensated, differential input, operational amplifiers with characteristics similar to the popular 741 type. To reduce the need for external bias circuitry the common mode range includes the negative power supply. This reduces the number of external components required for most applications. To eliminate crossover distortion, when operated from a split power supply, the output was designed for Class AB operation and can drive a capacitive load without instability.

The 835B will operate over a temperature range of -55°C to +125°C. For operation from 0°C to +70°C, the 835C should be used.

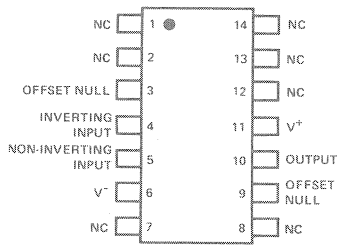
Connection Diagrams

L PACKAGE
14 LEAD CERDIP
(TOP VIEW)



Order Part Numbers:
835BL, 835CL

J PACKAGE
14 LEAD PLASTIC DIP
(TOP VIEW)



Order Part Number:
835J

*available soon

844/846 Series

(Formerly Teledyne 141/142 Series)

Operational Amplifiers

Features

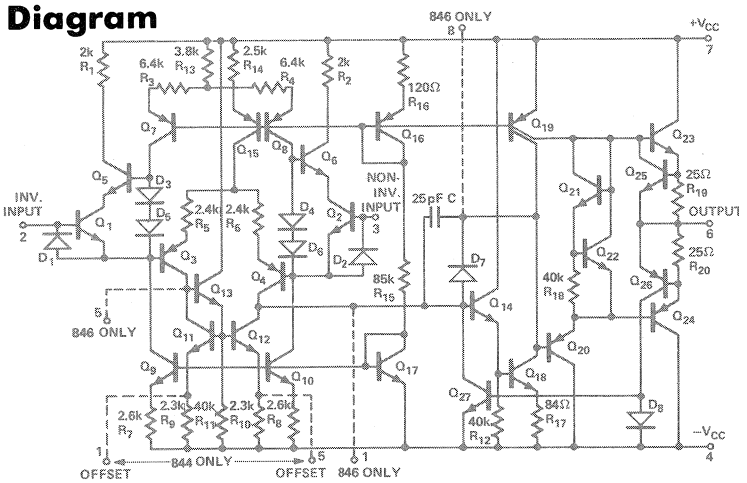
- GUARANTEED SLEW RATE – 1.0V/μs MIN.
- LOW INPUT BIAS CURRENT – 30nA MAX.
- LOW INPUT OFFSET CURRENT – 5nA MAX.
- LOW OFFSET VOLTAGE – 2mV MAX.
- LOW OFFSET VOLTAGE DRIFT – 15μV/°C

Description

The Teledyne Semiconductor 844B/846B Series are general purpose operational amplifiers constructed on a single monolithic silicon substrate using planar epitaxial techniques. They are high performance integrated circuits intended for a wide variety of general applications and also for applications where high slew rate and high input impedance are important. The 844B/846B series amplifiers may be used to increase system accuracy and extend the useful frequency range of existing designs in timer, integrator, sample and hold, D/A converters, and active filters. These designs are plug-in replacements for many popular operational amplifiers such as 741, 107, and 101 types.

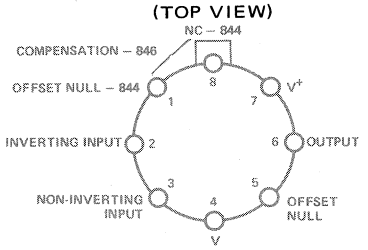
The 844B is internally compensated. The 846B is uncompensated allowing the designer the flexibility to individually tailor the frequency response to match the circuit application. The bandwidth of the 846B series can be extended with 2 pole or feed forward compensation.
(formerly Teledyne 141/142 Series)

Equivalent Circuit Diagram



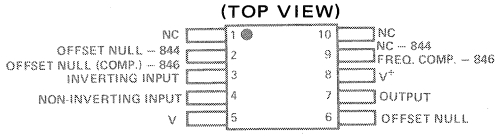
Connection Diagrams

E PACKAGE
8 LEAD METAL CAN
(TOP VIEW)



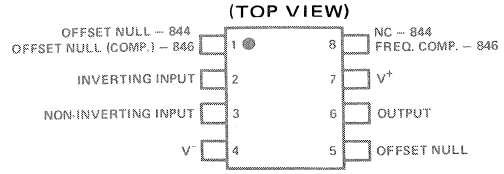
Order Part Numbers:
844BE, 844CE,
846BE, 846CE

H PACKAGE
10 LEAD FLATPACK
(TOP VIEW)



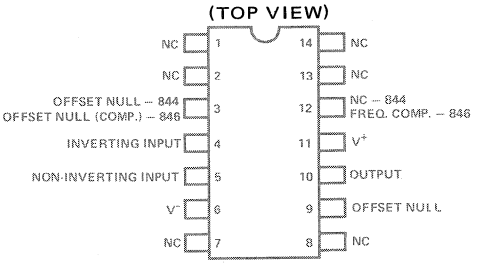
Order Part Numbers:
844BH, 846BH

P PACKAGE
8 LEAD PLASTIC MINIDIP
(TOP VIEW)



Order Part Numbers:
844CP, 846CP

L PACKAGE
14 LEAD CERDIP
(TOP VIEW)



Order Part Numbers:
844BL, 844CL,
846BL, 846CL

Absolute Maximum Ratings

	844B	844C
Input Voltage (Note 1)	±15V	±15V
Differential Input Voltage	±30V	±30V
Output Short Circuit Duration (Note 2)	Indefinite	Indefinite
Internal Power Dissipation (Note 3)		
Metal Can (E)	500mW	500mW
Ceramic Dual-In-Line (L)	670mW	670mW
Flatpack (H)	570mW	570mW
Supply Voltage	±22V	±18V
Storage Temperature Range	−65°C/+150°C	−65°C/+150°C
Operating Temperature Range	−55°C/+125°C	0°C/+70°C
Lead Soldering Temperature (60 sec.)	300°C	300°C
Junction Temperature	150°C	150°C

The above ratings are not meant to imply operation at each of these extremes simultaneously. Exceeding any or all of the absolute maximum ratings may cause permanent damage to the device.

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature (844B). Rating applies to +70°C case temperature or +55°C ambient temperature (844C).
3. Rating applies to ambient temperatures up to 75°C ambient. For operation above T_A = 75°C, derate linearly at 6.7mW/°C for the metal can, 8.9mW/°C for the ceramic dual-in-line, and 7.5mW/°C for the flatpack. For the flatpack, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16" thick epoxy-glass board with ten 0.03" wide, 2 oz. copper conductors.

Electrical Characteristics

Test Conditions

	T_{MIN}	T_{MAX}	V_S
844B	−55°C	+125°C	±5 to ±20V
844C	0°C	+70°C	±5 to ±15V

Unless Otherwise Noted

Parameter	844B Test Conditions		844B Min.	844B Typ.	844B Max.	844C Test Conditions		844C Min.	844C Typ.	844C Max.	Unit
Input Offset Voltage	$R_S \leq 50k\Omega$	25°C		1.0	2	25°C			3	5	mV
		T_{MIN} - T_{MAX}			3	0°C to 70°C				7.5	mV
Input Offset Current		25°C		0.7	5	25°C			3	10	nA
		T_{MIN} - T_{MAX}			10	0°C to 70°C				20	nA
Input Bias Current		25°C		12	30	25°C			40	75	nA
		T_{MIN} - T_{MAX}			60	0°C to 70°C				100	nA
Input Resistance		25°C	25	75		25°C		1.5	22		MΩ
Supply Current	V_S = ± 20V	25°C		2.5	3	V_S = ± 15V	25°C		2.5	3	mA
		T_{MAX}		2.0	2.5						
Large Signal Voltage Gain	V_S = ± 15V, V_{OUT} = ± 10V, $R_L \geq 2k\Omega$	25°C	100	300		V_S = ± 15V, V_{OUT} = ± 10V, $R_L \geq 2k\Omega$	25°C	50	300		V/mV
		T_{MIN} - T_{MAX}	40				0°C to 70°C	30			V/mV
Avg. Temperature Coefficient of Input Offset Voltage		T_{MIN} - T_{MAX}		3	15	0°C to 70°C			6	30	µV/°C
Avg. Temperature Coefficient of Input Offset Current	25°C ≤ T_A ≤ T_{MAX}			0.01	0.05	25°C ≤ T_A ≤ 70°C			0.01	0.2	nA/°C
	T_{MIN} ≤ T_A ≤ 25°C			0.02	0.1	0°C ≤ T_A ≤ 25°C			0.02	0.4	nA/°C
Output Voltage Swing	V_S = ± 15V	R_L = 10kΩ	±12	±13		V_S = ± 15V	R_L = 10kΩ	±12	±12.5		V
		R_L = 2kΩ	±10	±12.5			R_L = 2kΩ	±10	±12.5		V
Input Voltage Range	V_S = ± 20V	T_{MIN} - T_{MAX}	±15	±17		V_S = ± 15V	0°C to 70°C	±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	T_{MIN} - T_{MAX}	80	96		$R_S \leq 50k\Omega$ 0°C to 70°C		70	90		dB
Supply Voltage Rejection Ratio									96		dB
Slew Rate	V_S = ± 15V, R_L = 2kΩ, C_L = 100pF	25°C	1.0	2.0		V_S = ± 15V, R_L = 2kΩ	25°C	1.0	2.0		V/µs

Absolute Maximum Ratings

	846B	846C
Input Voltage (Note 1)	±15V	±15V
Differential Input Voltage	±30V	±30V
Output Short Circuit Duration (Note 2)	Indefinite	Indefinite
Internal Power Dissipation (Note 3)		
Metal Can (E)	500mW	500mW
Ceramic Dual-In-Line (L)	670mW	670mW
Flatpack (H)	570mW	570mW
Supply Voltage	±22V	±18V
Storage Temperature Range	−65°C/+150°C	−65°C/+150°C
Operating Temperature Range	−55°C/+125°C	0°C/+70°C
Lead Soldering Temperature (60 sec.)	300°C	300°C
Junction Temperature	150°C	150°C

The above ratings are not meant to imply operation at each of these extremes simultaneously. Exceeding any or all of the absolute maximum ratings may cause permanent damage to the device.

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature (846B). Rating applies to +70°C case temperature or +55°C ambient temperature (846C).
3. Rating applies to ambient temperatures up to 75°C ambient. For operation above T_A = 75°C, derate linearly at 6.7mW/°C for the metal can, 8.9mW/°C for the ceramic dual-in-line, and 7.5mW/°C for the flatpack. For the flatpack, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16" thick epoxy-glass board with ten 0.03" wide, 2 oz. copper conductors.

Electrical Characteristics

Test Conditions

	T_{MIN}	T_{MAX}	V_S	C_1
846B	−55°C	+125°C	±5 to ±20V	30pF
846C	0°C	+70°C	±5 to ±15V	30pF

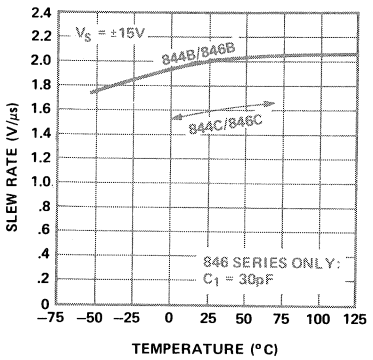
Unless Otherwise Noted

Parameter	846B Test Conditions		Min.	Typ.	Max.	846C Test Conditions		Min.	Typ.	Max.	Unit
Input Offset Voltage	$R_S \leq 50k\Omega$	25°C		1.0	2	25°C			3	5	mV
		T_{MIN} - T_{MAX}			3	0°C to 70°C				7.5	mV
Input Offset Current		25°C		0.7	5	25°C			3	10	nA
		T_{MIN} - T_{MAX}			10	0°C to 70°C				20	nA
Input Bias Current		25°C		12	30	25°C			40	75	nA
		T_{MIN} - T_{MAX}			60	0°C to 70°C				100	nA
Input Resistance		25°C	25	75		25°C		1.5	22		MΩ
Supply Current	V_S = ± 20V	25°C		2.5	3	V_S = ± 15V	25°C		2.5	3	mA
		T_{MAX}		2.0	2.5						
Large Signal Voltage Gain	V_S = ± 15V, V_{OUT} = ± 10V, $R_L \geq 2k\Omega$	25°C	100	300		V_S = ± 15V V_{OUT} = ± 10V $R_L \geq 2k\Omega$	25°C	50	300		V/mV
		T_{MIN} - T_{MAX}	40				0°C to 70°C	30			V/mV
Avg. Temperature Coefficient of Input Offset Voltage		T_{MIN} - T_{MAX}		3	15	0°C to 70°C			6	30	µV/°C
Avg. Temperature Coefficient of Input Offset Current	25°C ≤ T_A ≤ T_{MAX}			0.01	0.05	25°C ≤ T_A ≤ 70°C			0.01	0.2	nA/°C
	T_{MIN} ≤ T_A ≤ 25°C			0.02	0.1	0°C ≤ T_A ≤ 25°C			0.02	0.4	nA/°C
Output Voltage Swing	V_S = ± 15V	R_L = 10kΩ	± 12	± 13		V_S = ± 15V	R_L = 10kΩ	± 12	± 12.5		V
		R_L = 2kΩ	± 10	± 12.5			R_L = 2kΩ	± 10	± 12.5		V
Input Voltage Range	V_S = ± 20V	T_{MIN} - T_{MAX}	± 15	± 17		V_S = ± 15V	0°C to 70°C	± 12	± 13.5		V
Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	T_{MIN} - T_{MAX}	80	96		$R_S \leq 50k\Omega$ 0°C to 70°C		70	90		dB
Supply Voltage Rejection Ratio									96		dB
Slew Rate	V_S = ± 15V R_L = 2kΩ C_L = 100pF	25°C	1.0	2.0		V_S = ± 15V R_L = 2kΩ	25°C	1.0	2.0		V/µs

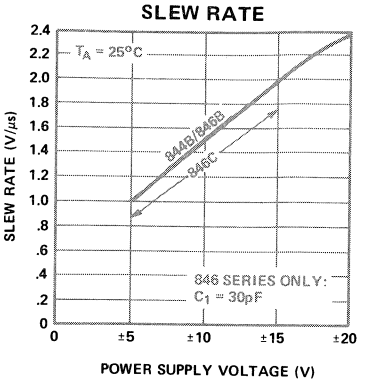
Typical Performance

844B/846B

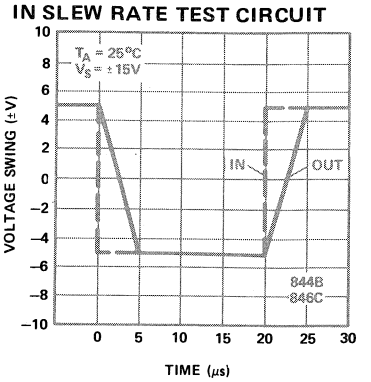
SLEW RATE



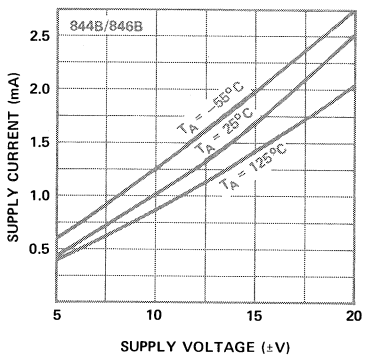
SLEW RATE



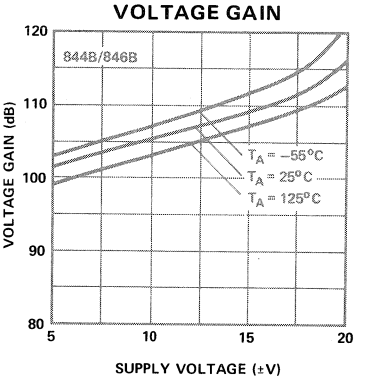
VOLTAGE FOLLOWER PULSE RESPONSE IN SLEW RATE TEST CIRCUIT



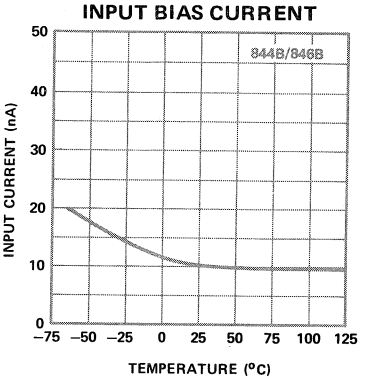
SUPPLY CURRENT



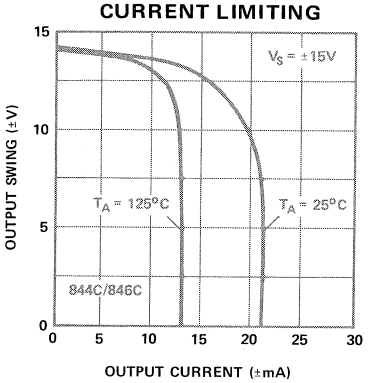
VOLTAGE GAIN



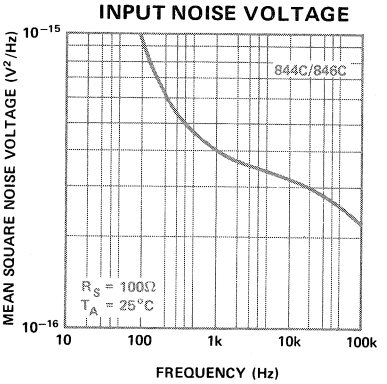
INPUT BIAS CURRENT



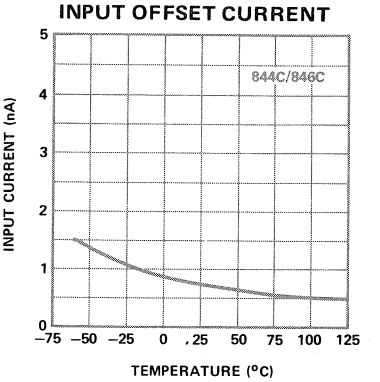
CURRENT LIMITING



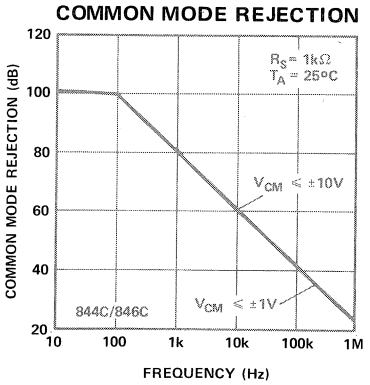
INPUT NOISE VOLTAGE



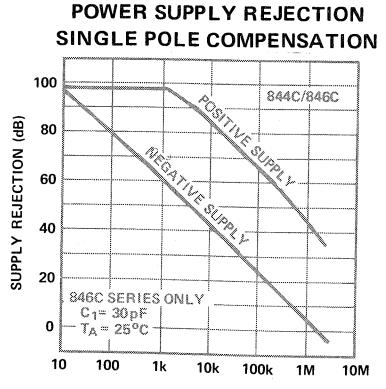
INPUT OFFSET CURRENT



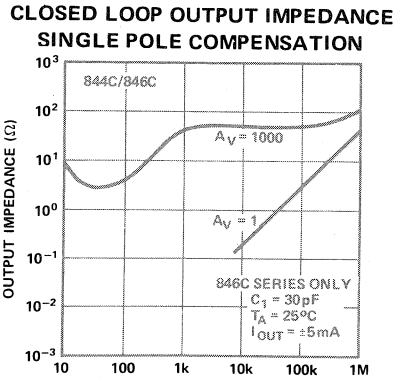
COMMON MODE REJECTION



POWER SUPPLY REJECTION SINGLE POLE COMPENSATION



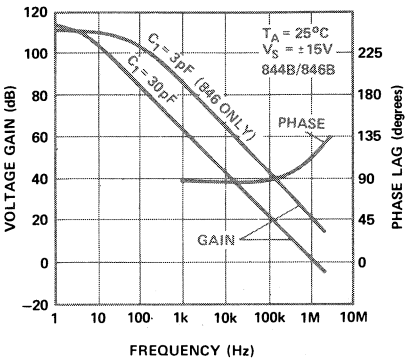
CLOSED LOOP OUTPUT IMPEDANCE SINGLE POLE COMPENSATION



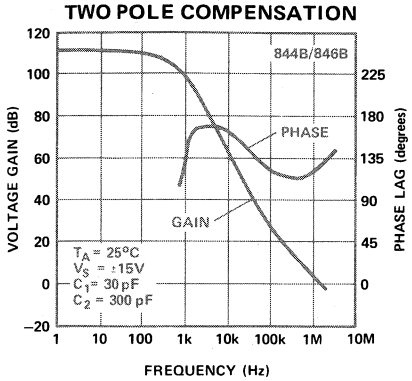
Typical Performance (Cont'd.)

844B/846B

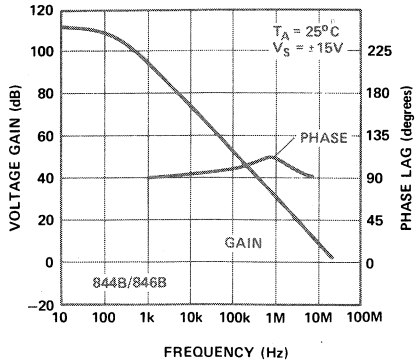
OPEN LOOP FREQUENCY RESPONSE
SINGLE POLE COMPENSATION



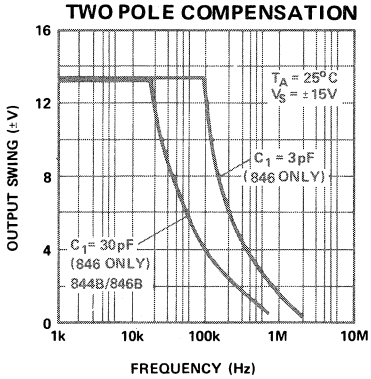
OPEN LOOP FREQUENCY RESPONSE
TWO POLE COMPENSATION



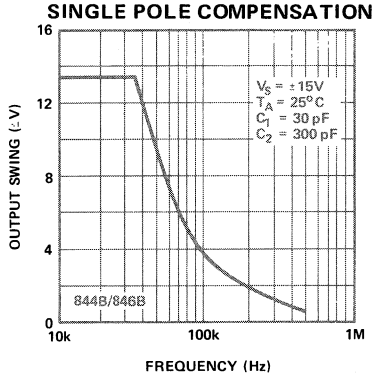
OPEN LOOP FREQUENCY RESPONSE
FEED FORWARD COMPENSATION



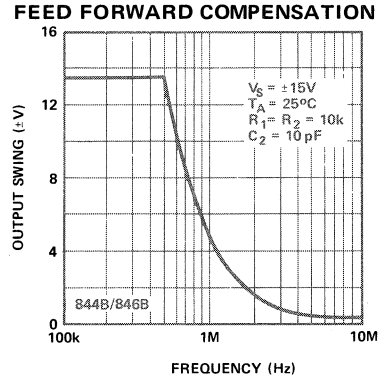
LARGE SIGNAL FREQUENCY RESPONSE
TWO POLE COMPENSATION



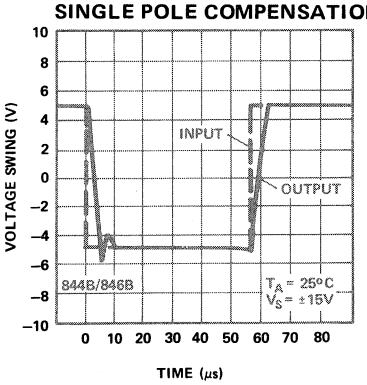
LARGE SIGNAL FREQUENCY RESPONSE
SINGLE POLE COMPENSATION



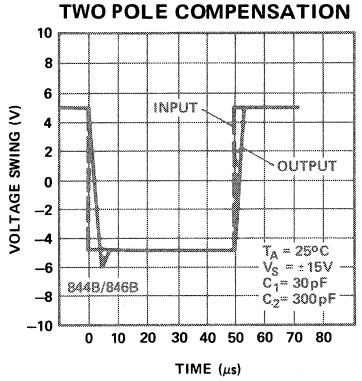
LARGE SIGNAL FREQUENCY RESPONSE
FEED FORWARD COMPENSATION



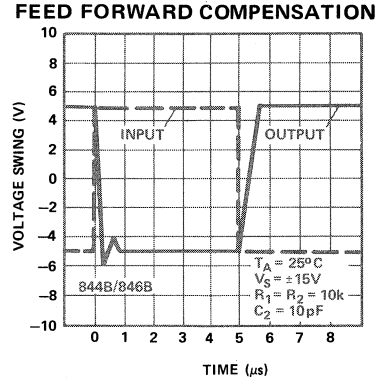
VOLTAGE FOLLOWER PULSE RESPONSE
SINGLE POLE COMPENSATION



VOLTAGE FOLLOWER PULSE RESPONSE
TWO POLE COMPENSATION



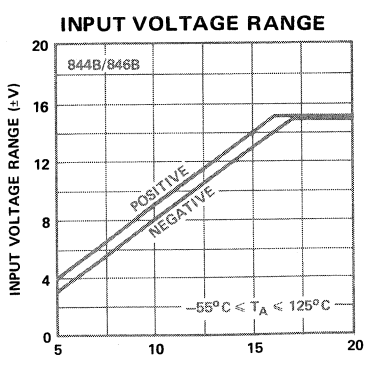
INVERTER PULSE RESPONSE
FEED FORWARD COMPENSATION



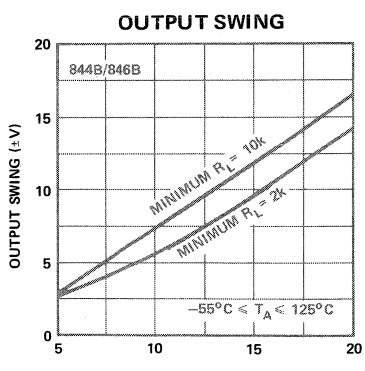
Guaranteed Performance

844B/846B

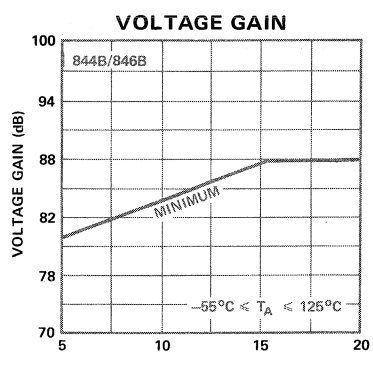
INPUT VOLTAGE RANGE



OUTPUT SWING



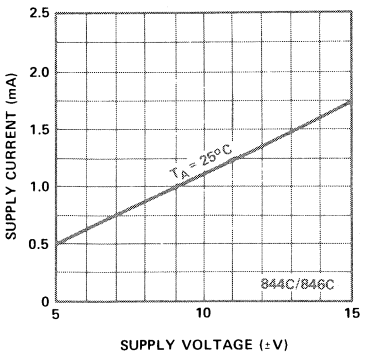
VOLTAGE GAIN



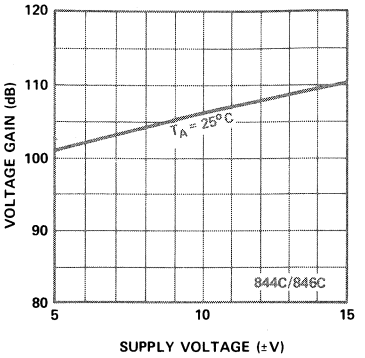
Typical Performance

844C/846C

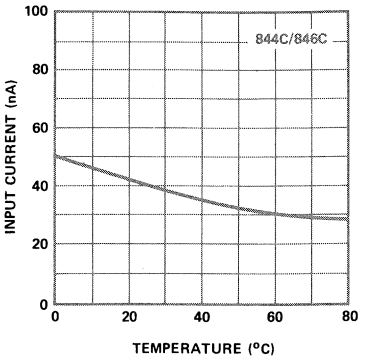
SUPPLY CURRENT



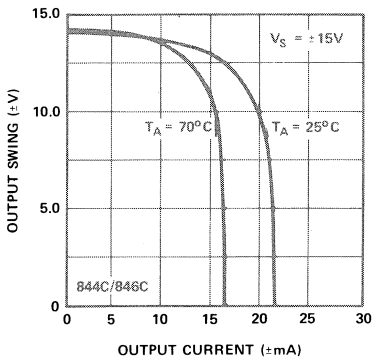
VOLTAGE GAIN



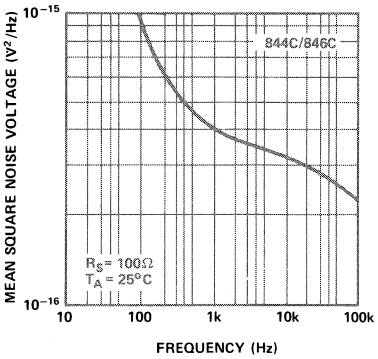
INPUT BIAS CURRENT



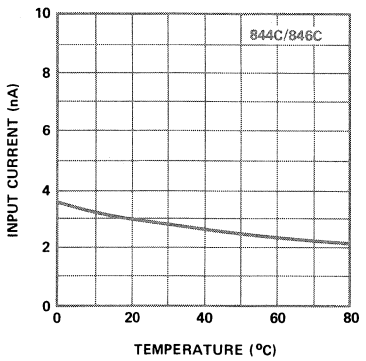
CURRENT LIMITING



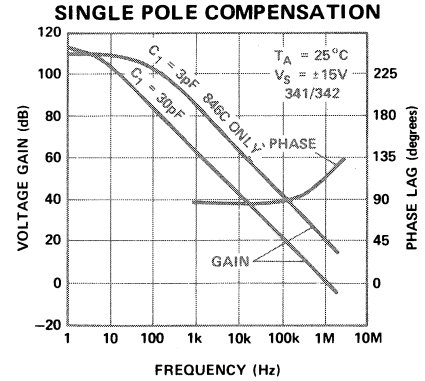
INPUT NOISE VOLTAGE



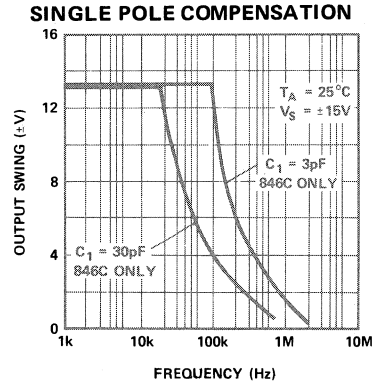
INPUT OFFSET CURRENT



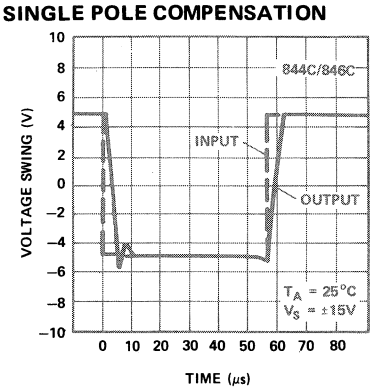
OPEN LOOP FREQUENCY RESPONSE
SINGLE POLE COMPENSATION



LARGE SIGNAL FREQUENCY RESPONSE
SINGLE POLE COMPENSATION



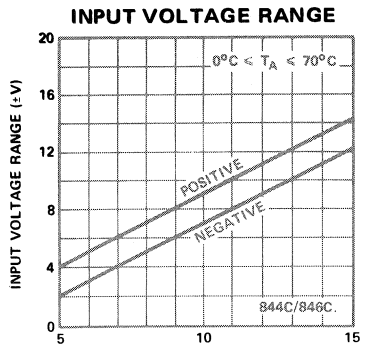
VOLTAGE FOLLOWER PULSE RESPONSE
SINGLE POLE COMPENSATION



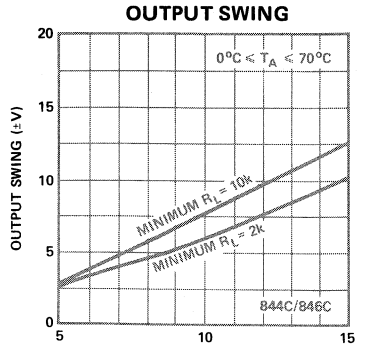
Guaranteed Performance

844C/846C

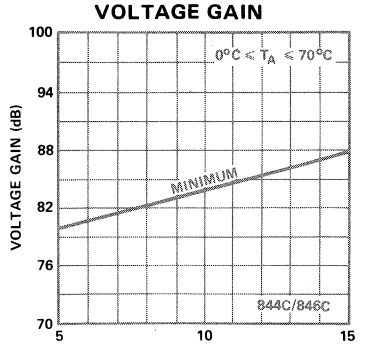
INPUT VOLTAGE RANGE



OUTPUT SWING

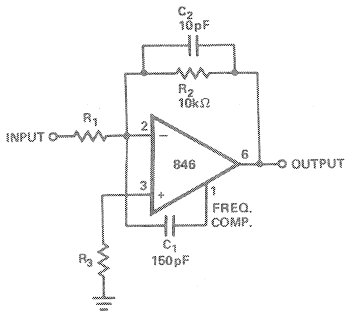


VOLTAGE GAIN

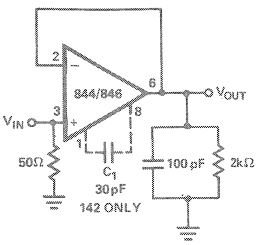


Test Circuits

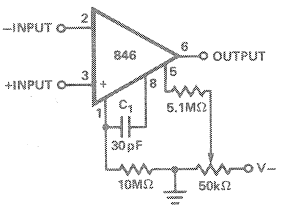
FEED FORWARD COMPENSATION



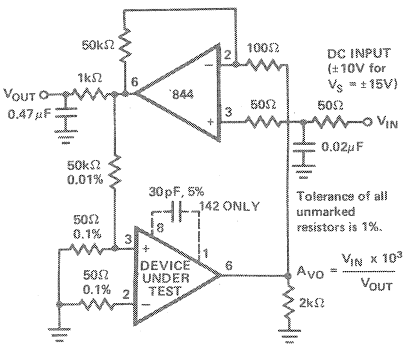
SLEW RATE TEST CIRCUIT



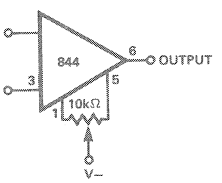
846 VOLTAGE OFFSET NULL



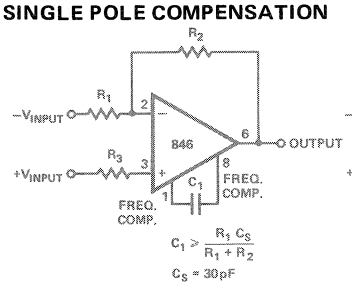
GAIN TEST CIRCUIT



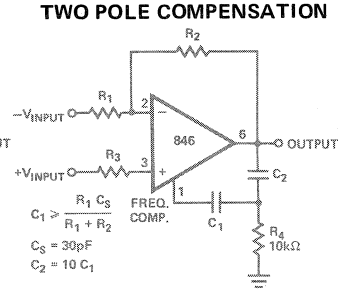
844 VOLTAGE OFFSET NULL



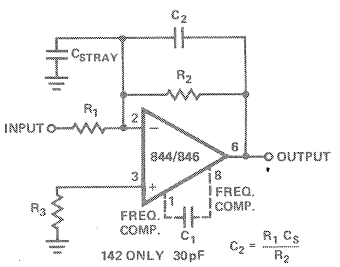
SINGLE POLE COMPENSATION



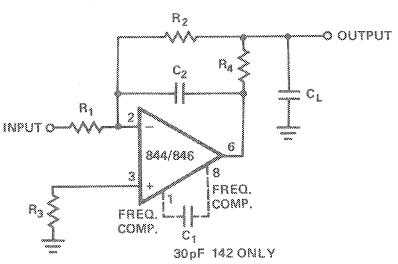
TWO POLE COMPENSATION



COMPENSATING FOR STRAY INPUT CAPACITANCE/LARGE FEEDBACK RESISTANCE



ISOLATING LARGE CAPACITIVE LOADS



The values given for the frequency compensation capacitor guarantee stability only for source resistances less than 10kΩ, stray capacitances on the summing junction less than 5pF and capacitive loads smaller than 100pF. If any of these conditions is not met, it is necessary to use a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors, or an RC network can be added to isolate capacitive leads.

Overload Protection Circuit

The 844B/846B series is designed for trouble free operation. However, experience has indicated that it is wise to observe certain precautions to protect the amplifiers from abnormal operating conditions. These precautions given here are applicable to practically any IC op amp.

If an input is driven from a low-impedance source, a limiting resistor, R_1, should be placed in series with the input lead to limit the peak instantaneous output current of the source to less than 100mA. This is especially important when the inputs go outside a piece of equipment where they could accidentally be connected to high voltage sources. Large capacitors on the input ($> 0.1 = \mu F$) should also be treated as low source impedances and isolated with resistors. Low impedance sources do not cause a problem unless their output voltage exceeds the supply voltage. However, the supplies go to zero when they are turned off, so the isolation is usually needed.

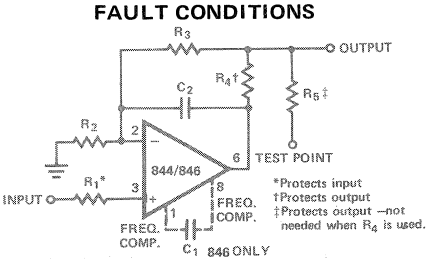
The 844B/846B series output circuitry is protected against damage from shorts to ground or to the power supplies by device design. However, when the amplifier output is connected to a test point, it should be isolated via limiting resistors R_4 or R_5, as test points frequently get shorted to power supplies that may exceed the rated operating voltages. Additionally, when the amplifier drives a load external to the equipment, it is also advisable to use a limiting resistor to preclude mishaps.

Precautions should also be taken to insure that the power supplies never become reversed even under transient conditions. With reverse voltages as low as 1V, the IC will conduct excessive current, fuzing internal metallization and damaging the device. If there is a possibility of this happening, clamp diodes with a high peak current rating should be connected to the device supply lines. Reversal of the voltage between V+ and V– will always cause a problem, and reversals with respect to ground may also cause difficulties.

Power supplies should be bypassed to ground at one point, minimum, on each circuit card. More bypass points should be considered for five or more amplifiers on a single card. For applications using feed-forward compensation, the power supply leads of each amplifier should be bypassed with low inductance capacitors because of the higher frequencies involved.

Pin connections shown are for H Package (TO-99).

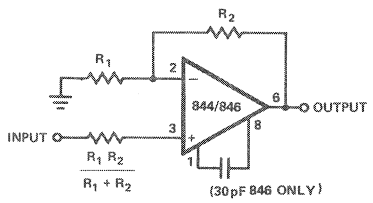
PROTECTING AGAINST GROSS FAULT CONDITIONS



Typical Applications

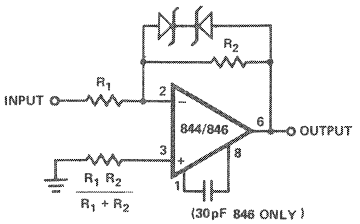
Amplifiers

NON-INVERTING AMPLIFIER



GAIN	R_1	R_2	B.W.	R_{IN}
10	1kΩ	9kΩ	150kHz	MΩ
100	100Ω	9.9kΩ	15kHz	MΩ
1000	100Ω	99.9kΩ	1.5kHz	MΩ

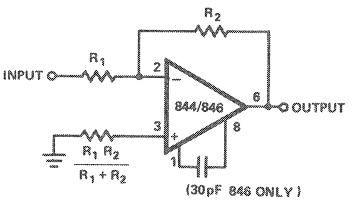
CLIPPING AMPLIFIER



$\frac{E_{out}}{E_{IN}} = \frac{R_2}{R_1}$ if $|E_{out}| << V_Z + 0.7V$

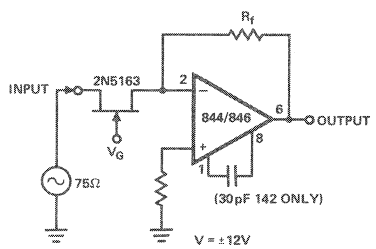
where V_Z = Zener breakdown voltage

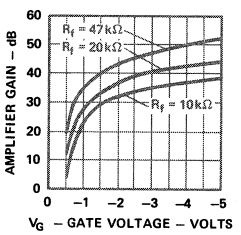
INVERTING AMPLIFIER



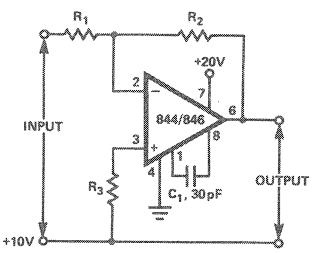
GAIN	R_1	R_2	B.W.	R_{IN}
1	10kΩ	10kΩ	1.5MHz	10kΩ
10	1kΩ	10kΩ	150kHz	1kΩ
100	1kΩ	100kΩ	15kHz	1kΩ
1000	100Ω	100kΩ	1.5kHz	100Ω

GAIN CONTROLLED AMPLIFIER

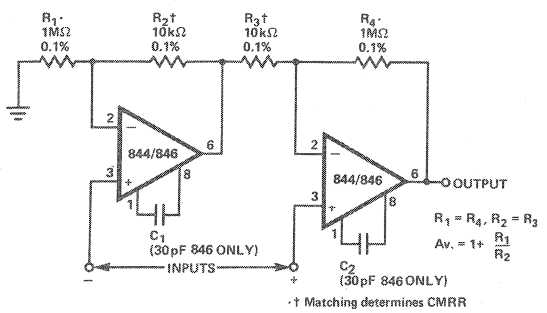




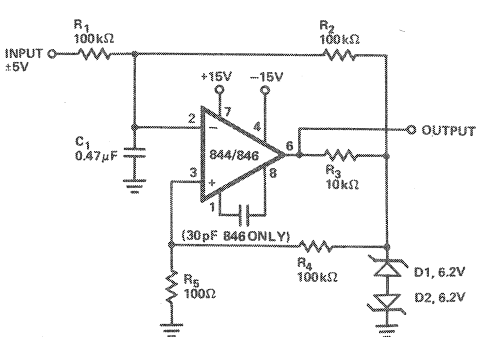
CIRCUIT FOR OPERATING WITHOUT A NEGATIVE SUPPLY



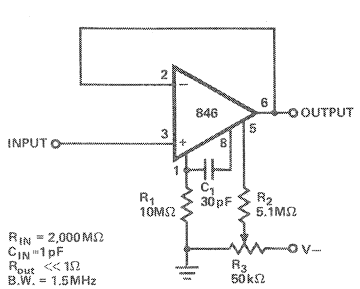
INSTRUMENTATION AMPLIFIER



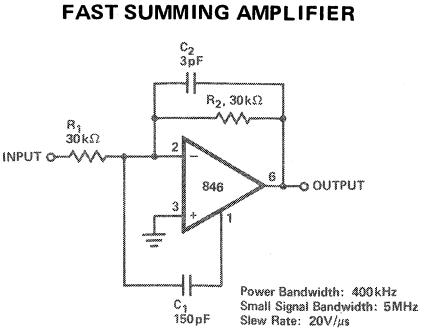
PULSE WIDTH MODULATOR



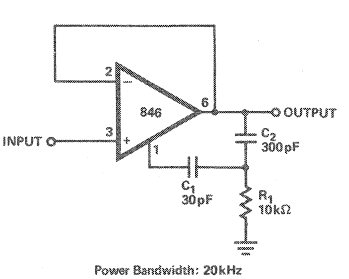
UNITY-GAIN VOLTAGE FOLLOWER WITH BALANCING CIRCUIT



FAST SUMMING AMPLIFIER



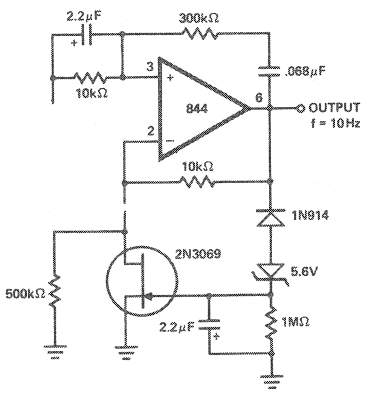
FAST VOLTAGE FOLLOWER



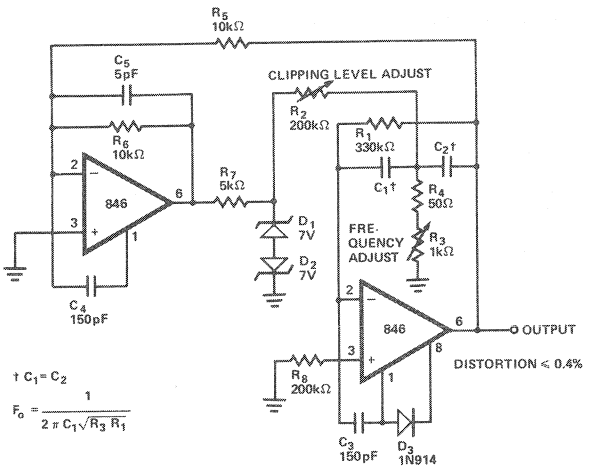
Typical Applications (Cont'd.)

Oscillators and Generators

844
LOW FREQUENCY WEIN BRIDGE SINE WAVE OSCILLATOR



846
LOW DISTORTION SINE WAVE OSCILLATOR

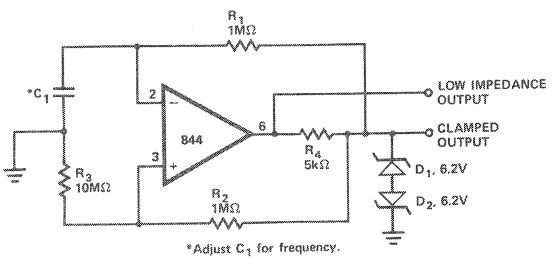


† $C_1 = C_2$

$$F_o = \frac{1}{2\pi C_1 \sqrt{R_3 R_1}}$$

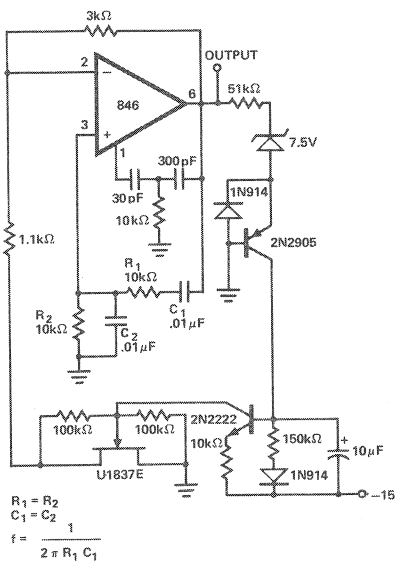
C_1, C_2	MINIMUM FREQUENCY	MAXIMUM FREQUENCY
0.47μF	18Hz	80Hz
0.1μF	80Hz	380Hz
0.022μF	380Hz	1.7kHz
0.0047μF	1.7kHz	8kHz
0.002μF	4.4kHz	20kHz

LOW FREQUENCY SQUARE WAVE GENERATOR



*Adjust C_1 for frequency.

WEIN BRIDGE OSCILLATOR WITH J-FET AMPLITUDE STABILIZATION

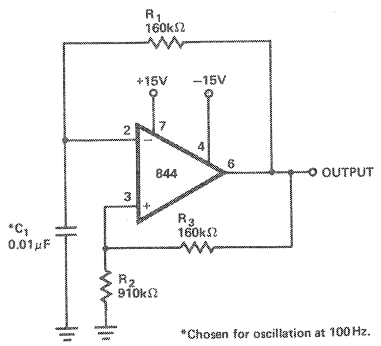


$R_1 = R_2$

$C_1 = C_2$

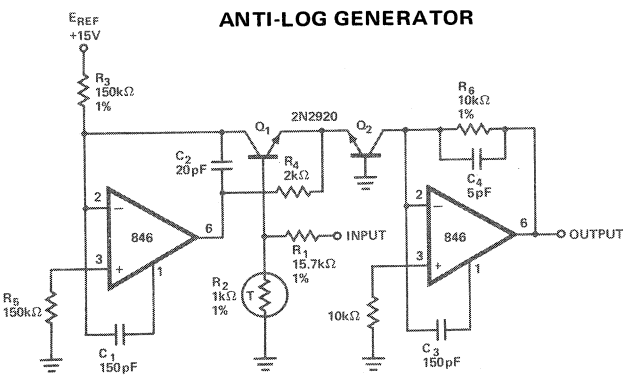
$$f = \frac{1}{2\pi R_1 C_1}$$

FREE-RUNNING MULTIVIBRATOR



*Chosen for oscillation at 100Hz.

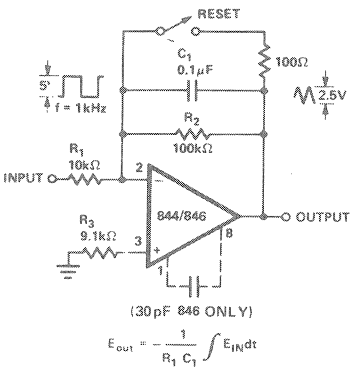
ANTI-LOG GENERATOR



Typical Applications (Cont'd.)

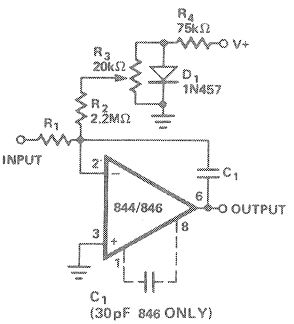
Integrators and Differentiators

SIMPLE INTEGRATOR



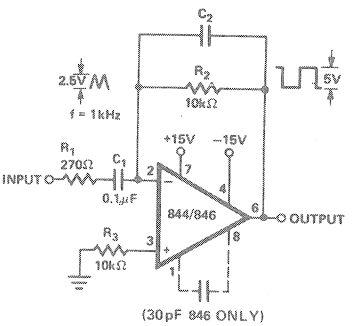
$$E_{out} = -\frac{1}{R_1 C_1}\int E_{IN}dt$$

INTEGRATOR WITH BIAS CURRENT COMPENSATION



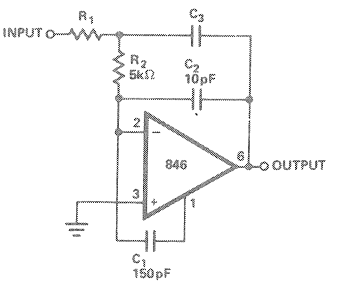
Adjust R_3 for zero integrator drift. Current drift typically 0.1nA/°C over −55°C to +125°C temperature range.

SIMPLE DIFFERENTIATOR



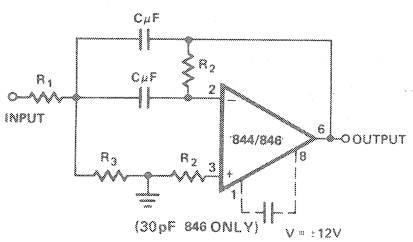
$$E_{out} = -R_2 C_1 \frac{dE_{IN}}{dt}$$

846 FAST INTEGRATOR



Filters and Tuned Circuits

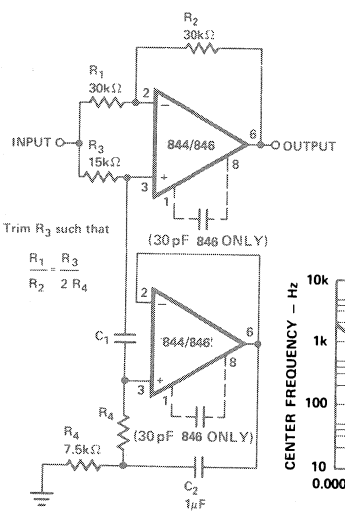
NOTCH FILTER USING THE 844 OR 846 AS A GYRATOR

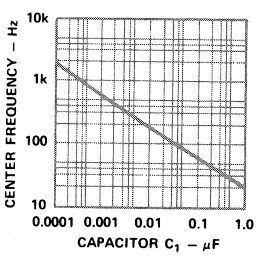


The values of the various components are given by:

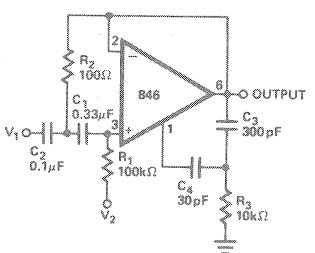
$$R_1 = \frac{1}{2\pi\Delta AC};\ R_2 = \frac{1}{\Delta\pi C};\ R_3 = \frac{1}{2\pi C\left[\frac{2f_o^2}{\Delta} - \Delta A\right]}$$

Where Δ is the 3dB bandwidth in Hz; A is the voltage gain and f_o is the center frequency.



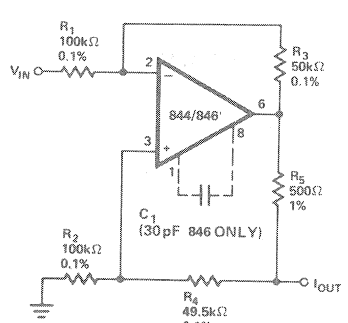


846 TUNED CIRCUIT



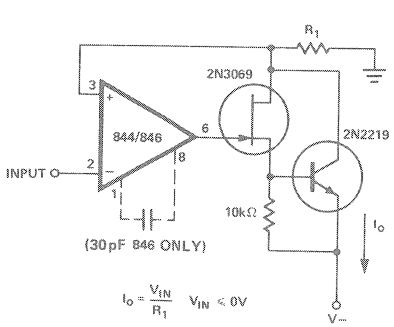
Current Sources and Monitors

BILATERAL CURRENT SOURCE



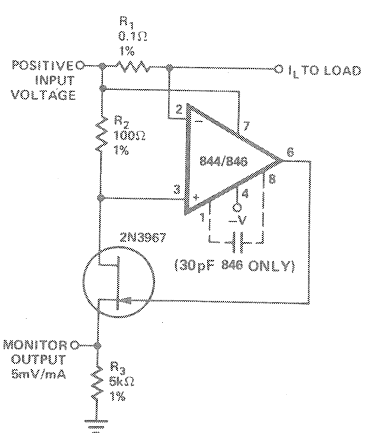
$$I_{OUT} = \frac{R_3 V_{IN}}{R_1 R_5} \qquad R_3 = R_4 + R_5,\ R_1 = R_2$$

PRECISION CURRENT SOURCE



$$I_o = \frac{V_{IN}}{R_1} \quad V_{IN} < 0V$$

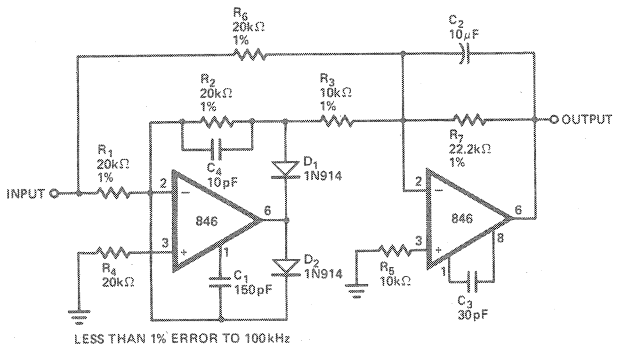
CURRENT MONITOR



Typical Applications (Cont'd.)

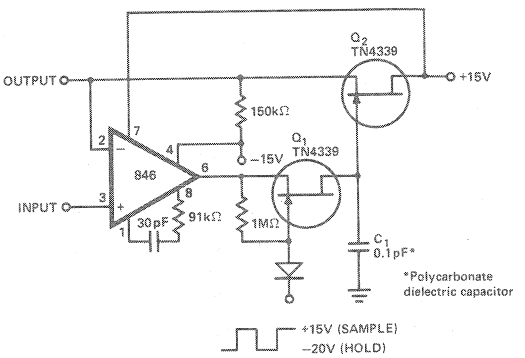
Other Circuits

PRECISION AC/DC CONVERTER

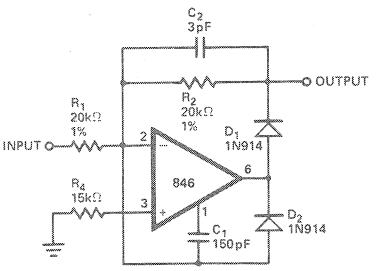


LESS THAN 1% ERROR TO 100kHz

LOW DRIFT SAMPLE AND HOLD



FAST HALF WAVE RECTIFIER



845 Series
Operational Amplifiers

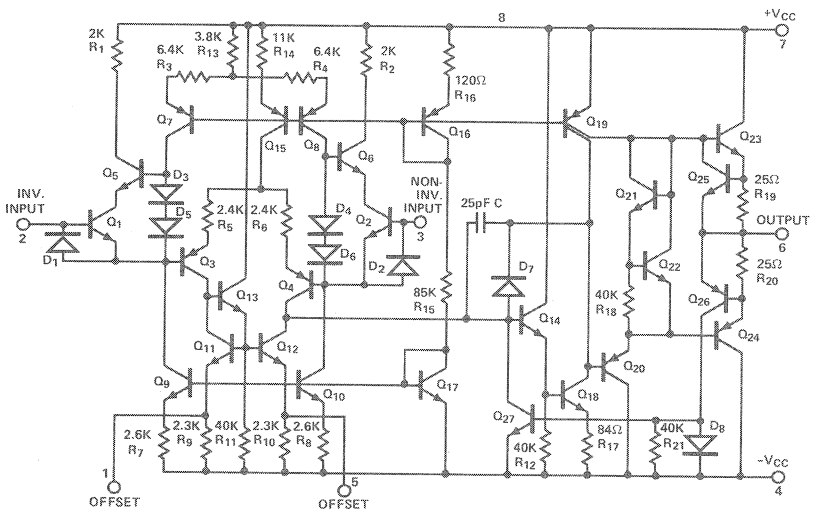
Features

- EASILY DRIVES 1000pF CAPACITIVE LOAD
- LOW INPUT BIAS CURRENT – 30nA MAX.
- LOW INPUT OFFSET CURRENT – 5nA MAX.
- LOW OFFSET VOLTAGE – 2mV MAX.
- LOW OFFSET VOLTAGE DRIFT – 15μV/°C
- INTERNAL FREQUENCY COMPENSATION

Description

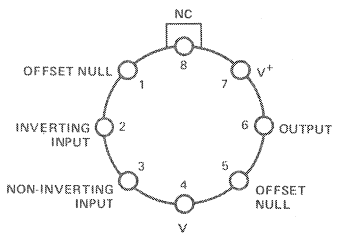
The Teledyne Semiconductor 845 Series are general purpose operational amplifiers constructed on a single monolithic silicon substrate using planar epitaxial techniques. They are high performance integrated circuits intended for a wide variety of general applications and also for applications where high input impedance is important. The 845 series amplifiers may be used to increase system accuracy of existing designs in timer, integrator, sample and hold, D/A converters, and active filters. These designs are plug-in replacements for many popular operational amplifiers such as 741, 107, and 101A types. The Teledyne 845 is especially useful in applications requiring excellent amplifier input characteristics plus the ability to drive high capacitance loads. For typical performance characteristics, refer to Teledyne 844/846 data sheets.

Equivalent Circuit Diagram



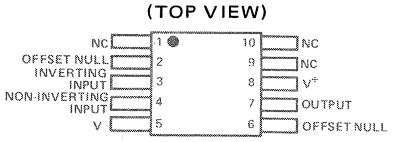
Connection Diagrams

E PACKAGE
8 LEAD METAL CAN
(TOP VIEW)



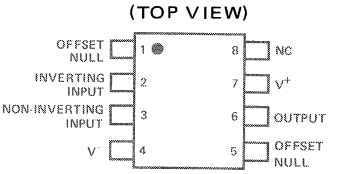
Order Part Numbers:
843BE
843CE

H PACKAGE
10 LEAD FLATPACK
(TOP VIEW)



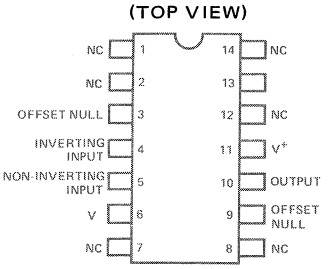
Order Part Numbers:
843BH

N PACKAGE
8 LEAD PLASTIC MINIDIP
(TOP VIEW)



Order Part Number:
LM344N

L PACKAGE
14 LEAD CERDIP
(TOP VIEW)



Order Part Numbers:
843BL
843CL

Absolute Maximum Ratings

	845B	845C
Input Voltage (Note 1)	±15V	±15V
Differential Input Voltage	±30V	±30V
Output Short Circuit Duration (Note 2)	Indefinite	Indefinite
Internal Power Dissipation		
Metal Can (E)	500mW	500mW
Ceramic Dual-In-Line (L)	670mW	670mW
Flatpack (H)	570mW	570mW
Supply Voltage	±22V	±18V
Storage Temperature Range	−65°C/+150°C	−65°C/+150°C
Operating Temperature Range	−55°C/+125°C	0°C/+70°C
Lead Soldering Temperature (60 sec.)	300°C	300°C
Junction Temperature	150°C	150°C

The above ratings are not meant to imply operation at each of these extremes simultaneously. Exceeding any or all of the absolute maximum ratings may cause permanent damage to the device.

NOTES:

1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature (844B). Rating applies to +70°C case temperature or +55°C ambient temperature (843C).
3. Rating applies to ambient temperatures up to 75°C ambient. For operation above T_A = 75°C, derate linearly at 6.7mW/°C for the metal can, 8.9mW/°C for the ceramic dual-in-line, and 7.5mW/°C for the flatpack. For the flatpack, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16" thick epoxy-glass board with ten 0.03" wide, 2 oz. copper conductors.

Electrical Characteristics

Test Conditions

	T_{MIN}	T_{MAX}	V_S	
845B	−55°C	+125°C	±5 to ±20V	Unless Otherwise Noted
845C	0°C	+70°C	±5 to ±15V	

PARAMETER	845B TEST CONDITIONS		MIN.	TYP.	MAX.	845C TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	$R_S \leq 50k\Omega$	25°C		1.0	2	25°C			3	5	mV
		T_{MIN} - T_{MAX}			3	0°C to 70°C				7.5	mV
Input Offset Current		25°C		0.7	5	25°C			3	10	nA
		T_{MIN} - T_{MAX}			10	0°C to 70°C				20	nA
Input Bias Current		25°C		12	30	25°C			40	75	nA
		T_{MIN} - T_{MAX}			60	0°C to 70°C				100	nA
Input Resistance		25°C	25	75		25°C		1.5	22		MΩ
Supply Current	V_S = ±20V	25°C		2.5	3	V_S = ±15V	25°C		2.5	3	mA
		T_{MAX}		2.0	2.5						
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L \geq 2k\Omega$	25°C	100	300		V_S = ±15V V_{OUT} = ±10V $R_L \geq 2k\Omega$	25°C	50	300		V/mV
		T_{MIN} - T_{MAX}	40				0°C to 70°C	30			V/mV
Avg. Temperature Coefficient of Input Offset Voltage		T_{MIN} - T_{MAX}		3	15	0°C to 70°C			6	30	µV/°C
Avg. Temperature Coefficient of Input Offset Current	25°C ≤ T_A ≤ T_{MAX}			0.01	0.05	25°C ≤ T_A ≤ 70°C			0.01	0.2	nA/°C
	T_{MIN} ≤ T_A ≤ 25°C			0.02	0.1	0°C ≤ T_A ≤ 25°C			0.02	0.4	nA/°C
Output Voltage Swing	V_S = ±15V	R_L = 10kΩ	±12	±13		V_S = ±15V	R_L = 10kΩ	±12	±12.5		V
		R_L = 2kΩ	±10	±12.5			R_L = 2kΩ	±10	±12.5		V
Input Voltage Range	V_S = ±20V	T_{MIN} - T_{MAX}	±15	±17		V_S = ±15V	0°C to 70°C	±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	T_{MIN} - T_{MAX}	80	96		$R_S \leq 50k\Omega$ 0°C to 70°C		70	90		dB
Supply Voltage Rejection Ratio									96		dB
Slew Rate	V_S = ±15V R_L = 2kΩ C_L = 100pF	25°C		.5		V_S = ±15V R_L = 2kΩ	25°C		.5		V/µs

1558/1458/1458C
Dual Operational Amplifiers

Features

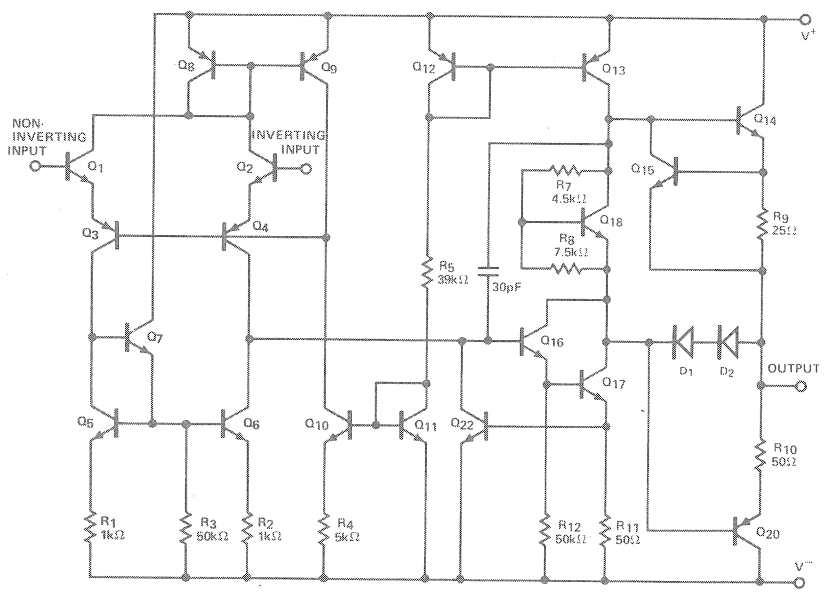
- SHORT-CIRCUIT PROTECTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGE
- LOW POWER CONSUMPTION
- NO LATCH-UP
- NO FREQUENCY COMPENSATION REQUIRED

Description

The Teledyne 1558 is a dual 741 general purpose operational amplifier constructed on a single monolithic chip. Frequency compensation is provided internally, insuring closed-loop stability. High common-mode voltage range and freedom from latch-up make the device useful as a voltage follower. Its high gain and its ability to operate with a wide range of supply voltage provide for excellect performance in summing amplifier, integrator, and general feedback applications.

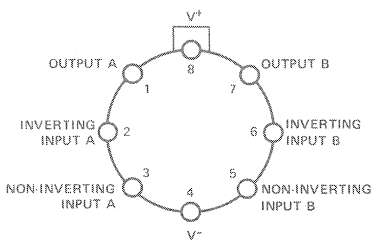
The 1458 and 1458C are identical to the 1558 except that the operating temperature range and electrical parameters are specified for industrial and commercial applications respectively. For Typical Characteristics and Applications, see Teledyne 747 data sheet.

Equivalent Circuit Diagram (Each Side)



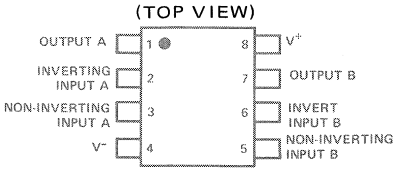
Connection Diagrams

E PACKAGE
8 LEAD METAL CAN
(TOP VIEW)



Order Part Numbers:
1558E (−55°C/+125°C)
1458E (0°C/+75°C)
1458CE (0°C/+75°C)

P PACKAGE
8 LEAD MINIDIP
(TOP VIEW)



Order Part Numbers:
1458P (0°C/+75°C)
1458CP (0°C/+75°C)

Absolute Maximum Ratings

	1558	1458/1458C
Differential Input Voltage (Note 1)	±30V	±30V
Common-Mode Input Voltage (Note 2)	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous
Power Supply Voltage	±22V	±18V
Internal Power Dissipation (Note 3)		
Metal Can (E)	830mW	830mW
Plastic Minidip (P)		780mW
Operating Temperature Range	-55°C/+125°C	0°C/+75°C
Storage Temperature Range	-65°C/+150°C	-65°C/+150°C

Electrical Characteristics (V^+ = +15 Vdc, V^- = −15 Vdc, T_A = +25°C unless otherwise noted)

Parameter	Conditions	Symbol	1558 Min	1558 Typ	1558 Max	1458 Min	1458 Typ	1458 Max	1458C Min	1458C Typ	1458C Max	Units
Input Bias Current	T_A = +25°C (See Note 4)	I_b		0.1	0.5		0.1	0.5		0.1	0.7	µAdc
	T_A = T_{low} to T_{high} (See Note 3)	I_b			1.5			0.8			1.0	
Input Offset Current	T_A = +25°C	I_{io}		0.01	0.2		0.01	0.2		0.01	0.3	µAdc
	T_A = T_{low} to T_{high}	I_{io}			0.5			0.3			0.4	
Input Offset Voltage	(R_S ≤ 10 kΩ) T_A = +25°C	V_{io}		1.0	5.0		2.0	6.0		2.0	10	mVdc
	T_A = T_{low} to T_{high}	V_{io}			6.0			7.5			12	
Differential Input Impedance	(Open-Loop, f = 20 Hz)											
Parallel Input Resistance		R_p	0.3	1.0		0.3	1.0			1.0		Megohms
Parallel Input Capacitance		C_p		6.0			6.0			6.0		pF
Common-Mode Input Impedance	(f = 20 Hz)	$Z_{(in)}$		200			200			200		Megohms
Common-Mode Input Voltage Swing		CMV_{in}	±12	±13		±12	±13		±11	±13		V_{pk}
Equivalent Input Noise Voltage	(A_V = 100, R_s = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz)	e_n		45			45			45		nV/(Hz)½
Common-Mode Rejection Ratio	(f = 100 Hz)	CM_{rej}	70	90		70	90		60	90		dB
Open-Loop Voltage Gain												
(V_o = ±10V,	T_A = +25°C	A_{VOL}	50,000	200,000		20,000	100,000					V/V
R_L = 2.0 k ohms)	T_A = T_{low} to T_{high}		25,000			15,000						
(V_o = ±10V, R	T_A = +25°C								20,000	100,000		
R_L = 10 k ohms)	T_A = T_{low} to T_{high}								15,000			
Power Bandwidth	(A_V = 1, R_l = 2.0 k ohms, THD ≤ 5%, V_o = 20V p-p)	P_{BW}		14			14			14		kHz
Unity Gain Crossover Frequency (open-loop)		f_c		1.1			1.1			1.1		MHz
Phase Margin (open-loop, unity gain)				65			65			65		degrees
Gain Margin				11			11			11		dB
Slew Rate (Unity gain)		dV_{out}/dt		0.8			0.8			0.8		V/µs
Transient Response (Unity gain)												
Risetime	V_{IN} = 20 mV, R_L = 2 kΩ,			0.35			0.35			0.35		µsec
Overshoot	C_L ≤ 100 pF			10			10			10		%
Output Impedance	(f = 20 Hz)	Z_{out}		75			75			75		ohms
Short-Circuit Output Current		I_{SC}		25			25			25		mAdc
Output Voltage Swing	(R_L = 10 k ohms)	V_o	±12	±14		±12	±14		±11	±14		Vpk
	R_L = 2 k ohms (T_A = T_{low} to T_{high})	V_o	±10	±13		±10	±13		±9.0	±13		
Average Temperature Coefficient of Input Offset Voltage	(R_S = 50 ohms T_A = T_{low} to T_{high})	TCV_{io}		15			15			15		µV/°C
Power Supply Sensitivity	V^- = constant, R_s ≤ 10 k ohms	S+		30	150		30	150		30		µV/V
	V^+ = constant, R_s ≤ 10 k ohms	S−		30	150		30	150		30		
Power Supply Current		I_D^+		2.3	5.0		2.3	5.6		2.3	8.0	mAdc
		I_D^-		2.3	5.0		2.3	5.6		2.3	8.0	
DC Quiescent Power Dissipation	(V_o = 0)	P_D		70	150		70	170		70	240	mW

NOTES:
1. For supply voltages of less than ±15V, the maximum differential input voltage is equal to ±(V^+ + [V^-]).
2. For supply voltages of less than ±15V, the maximum input voltage is equal to the supply voltage (+V^+, − [V^-]).
3. Ratings are based on a maximum junction temperature of 150°C. For operation above 25°C ambient, derate by 6.7mW/°C for the metal can, and 6.3mW/°C for the plastic package.
4. T_{low}: 0°C for 1458 and 1458C, −55°C for 1558. T_{high}: +75°C for 1458 and 1458C, +125°C for 1558.

2740
FET Input Operational Amplifiers

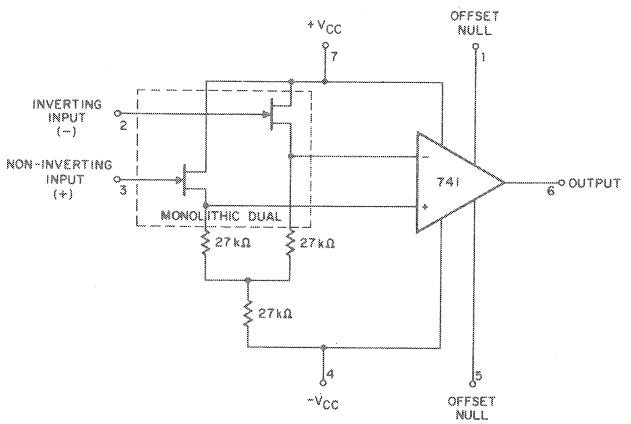
Features

- HIGH INPUT IMPEDANCE
- HIGH GAIN
- LARGE COMMON MODE REJECTION OVER WIDE INPUT VOLTAGE RANGE
- LOW POWER DISSIPATION

Description

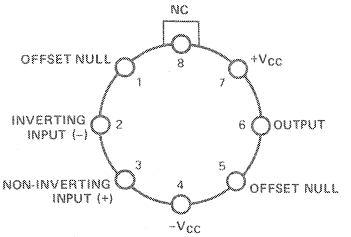
The Teledyne Semiconductor 2740 operational amplifier combines the superior performance of the widely accepted 741 operational amplifier with the high input impedance characteristics of a monolithic dual field effect transistor stage. It is intended for use in applications requiring extremely low bias and offset currents such as high impedance filter sections and integrators. Equally versatile in general feedback applications, the 2740 incorporates output short-circuit protection, input overvoltage and "latch-up" immunity, internal 6 dB/octave frequency compensation, external offset voltage null capability, and has the same pin configuration as the 741.

Equivalent Circuit Diagram



Connection Diagram

E PACKAGE
8 LEAD METAL CAN
(TOP VIEW)



Order Part Numbers:
2740BE, 2740CE,
2740DE

Absolute Maximum Ratings

	2740B	2740C	2740D
Supply Voltage	±22V	±22V	±22V
Input Voltage (Note 1)	±15V	±15V	±15V
Differential Input Voltage (Note 1)	30V	30V	30V
Power Dissipation (Note 2)	800mW	800mW	800mW
Output Short Circuit Duration (Note 3)	Indefinite	Indefinite	Indefinite
Storage Temperature	−65°C/+150°C	−65°C/+150°C	−65°C/+150°C
Operating Temperature Range	−55°C/+125°C	0°C/+100°C	0°C/+100°C
Lead Soldering Temperature 1/16" from Case, 10 seconds max.	300°C	300°C	300°C

NOTES:

1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies for case temperatures up to the maximum operating temperature. Derate linearly at 10.7mW/°C for ambient temperature above +75°C.
3. Short circuit may be to ground or either supply. Rating applies for case temperature up to the maximum operating temperature or +75°C ambient temperature.
4. When using high impedance operational amplifiers, be sure to adequately decouple the power supplies.

Electrical Characteristics V_{CC} = ±15V, T_A = 25°C

PARAMETER	TEST FIG	TEST CONDITIONS	SYMBOL	2740B MIN	2740B TYP	2740B MAX	2740C MIN	2740C TYP	2740C MAX	2740D MIN	2740D TYP	2740D MAX	UNITS
Open Loop Voltage Gain	1	R_S = 0, $R_L \geq$ 2KΩ V_{in} = ±10V	A_O	90	94		90	94		86	90		dB
Input Offset Voltage	1	R_S = 1MΩ V_{in} = 0	V_{OS}		3	5		5	10		10	20	mV
Input Bias Current	2	V_{in} = 0	I_B		10	50		10	50		20	50	pA
Input Offset Current	2	V_{in} = 0	I_{OS}		5	25		5	25		10	25	pA
Input Resistance	2	V_{in} = ±10V	R_{in}	100	200		100	200		50	100		KmΩ
Common Mode Voltage Range	3	CMRR Test Condition	CMVR	±10			±10			±10			V_{pk}
Common Mode Rejection Ratio	3	Common Mode Input = ±10V peak	CMRR	60	80		60	80		60	80		dB
Power Supply Rejection Ratio	1	V_{in} = 0, R_S = 1MΩ ΔV_{CC} = ±1V, each Supply Independent	PSRR	60	80		60	80		60	80		dB
Output Voltage Swing	4	V_{in} = ±10V, $R_L \geq$ 2KΩ $C_L \leq$ 100pF	V_O	±10			±10			±10			V_{pk}
Power Dissipation	4	V_{in} = 0V $R_L \geq$ 2KΩ $C_L \leq$ 100pF	P_{DISS}		80	90		80	90		90	100	mW
V_{CC} = ±15V, T_A = T_{MIN} to T_{MAX} unless otherwise noted.													
Open Loop Voltage Gain	1	R_S = 0, $R_L \geq$ 2KΩ V_{in} = ±10V	A_O	86	90		86	90		80	84		dB
Input Bias Current	2	V_{in} = 0, T_A = T_{MAX} only	I_B		1	10		1	10		1	10	nA
Input Offset Current	2	V_{in} = 0, T_A = T_{MAX} only	I_{OS}		0.5	5		0.5	5		0.5	5	nA
Common Mode Voltage Range	3	CMRR Test Condition	CMRV	±10			±10			±10			V_{pk}
Common Mode Rejection Ratio	3	Common Mode Input = ±10V peak	CMRR	60	74		60	74		60	74		dB
Power Supply Rejection Ratio	1	V_{in} = 0, R_S = 1KΩ ΔV_{CC} = ±1V, each Supply Independent	PSRR	60	74		60	74		60	74		dB

Electrical Characteristics (Cont'd.) $V_{CC} = \pm 15V$, $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	TEST FIG	TEST CONDITIONS	SYMBOL	2740B			2740C			2740D			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Swing	4	$V_{in} = \pm 10V$, $R_L \geq 2K\Omega$ $C_L \leq 100pF$	V_O	±10			±10			±10			V_{pk}
Input Offset Voltage Drift	1	$V_{in} = 0$, $R_S = 1K\Omega$	$(\Delta V_{OS})_T$		5	10		5	10		5	15	mV
Power Dissipation	4	$V_{in} = 0$, $R_L \geq 2K\Omega$ $C_L \leq 100pF$	P_{DISS}		50	100		50	100		60	110	mW

Test Circuits

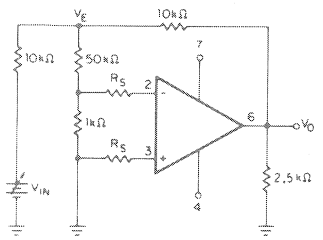


Fig. 1

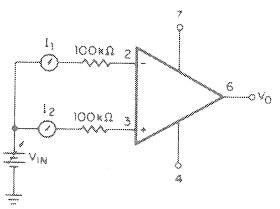


Fig. 2

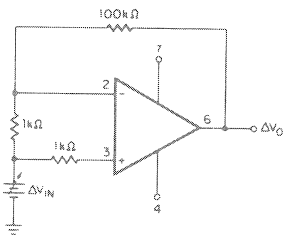


Fig. 3

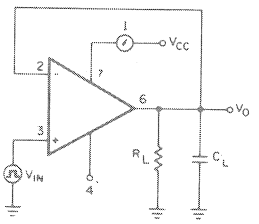


Fig. 4

$$A_O = 34\ dB + 20\ LOG \frac{\Delta V_O}{\Delta V_E}$$

$$V_{OS} = \frac{V_O}{112}$$

$$PSRR = 20\ LOG \frac{\Delta V_{OS}}{\Delta V_{CC}}$$

$$I_B = \frac{I_1 + I_2}{2}$$

$$I_{OS} = I_1 - I_2$$

$$R_{IN} = \frac{\Delta V_{IN}}{\Delta I_B}$$

$$(\Delta V_{OS})_T = |V_{OS}\ (T_A = MIN) - V_{OS}\ (T_A = MAX)|$$

$$CMRR = 40\ dB + 20\ LOG \left[\frac{\Delta V_{IN}}{\Delta V_{IN} - \Delta V_O} \right]$$

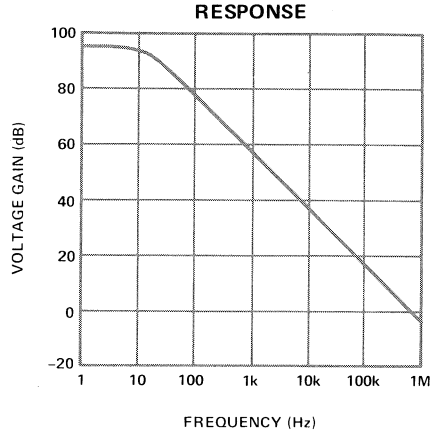
$$P_{DISS} = 2\ V_{CC} \times I$$

$$OS = 100 \frac{V_{MAX} - V_{IN}}{V_{IN}}\ \%$$

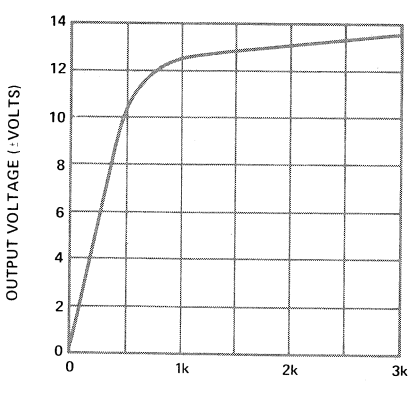
$$\frac{dV_O}{dt} = 10\% - 90\%\ V_O$$

Typical Characteristics

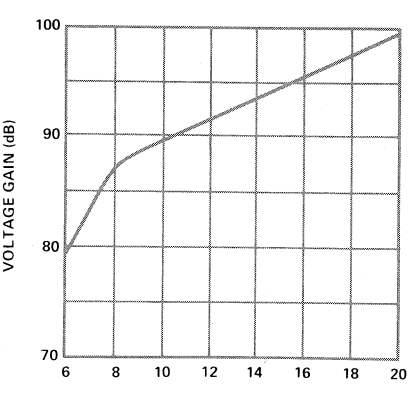
OPEN LOOP FREQUENCY RESPONSE



OUTPUT SWING

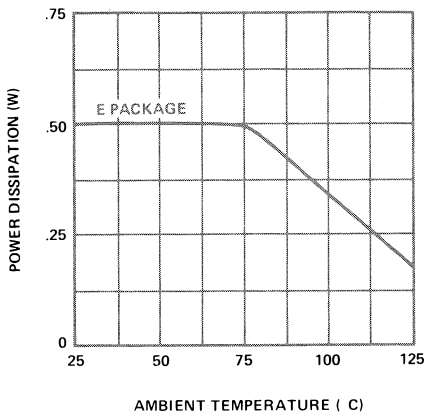


OPEN LOOP VOLTAGE GAIN

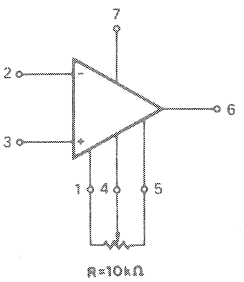


Typical Characteristics (Cont'd.)

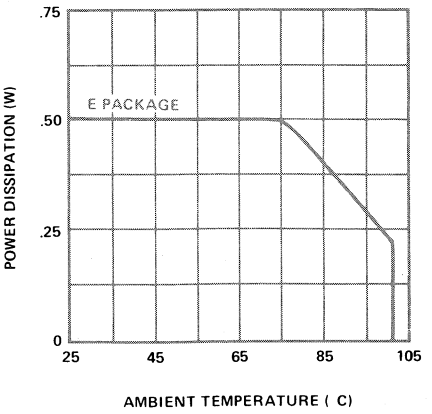
"B" DISSIPATION RATING



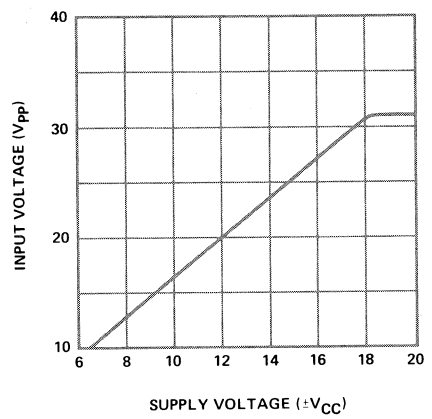
VOLTAGE OFFSET NULL CIRCUIT



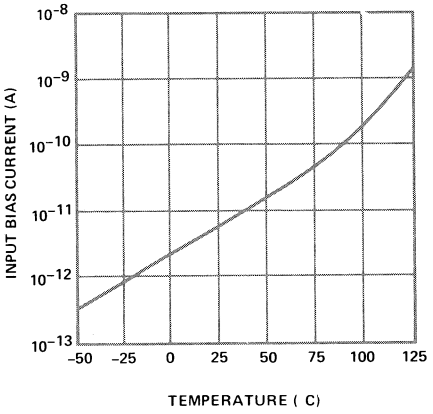
C&D DISSIPATION RATING



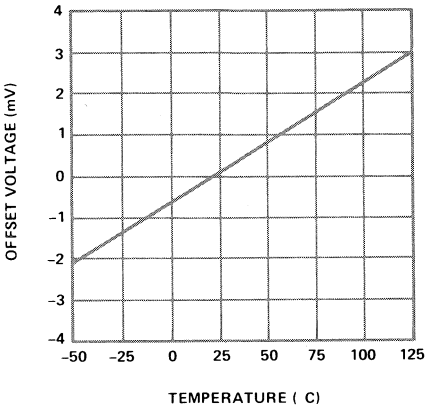
COMMON MODE VOLTAGE RANGE



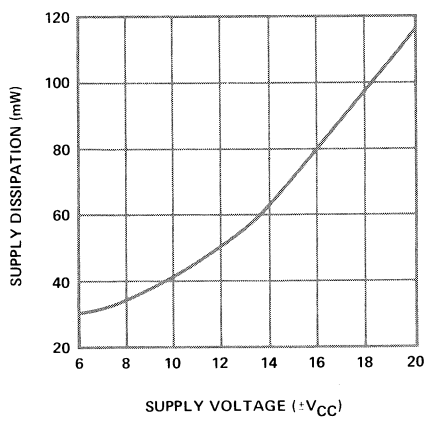
INPUT BIAS CURRENT



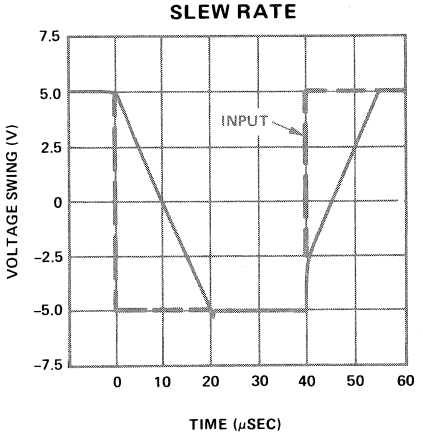
OFFSET VOLTAGE



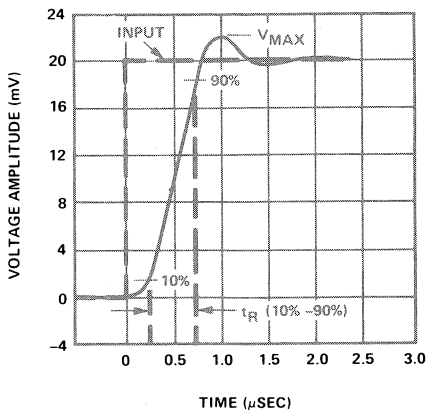
POWER SUPPLY CONSUMPTION



VOLTAGE FOLLOWER SLEW RATE

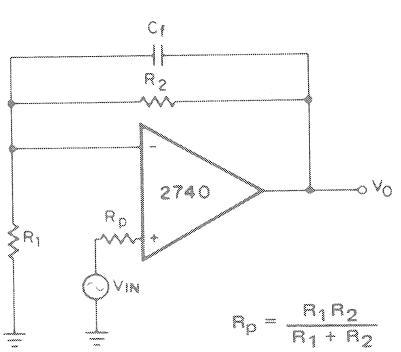


TRANSIENT RESPONSE



Typical Applications

To insure a maximum phase margin when large inverting input source resistors are employed, an external feedback capacitance, C_f, is recommended to compensate for feedback lag due to the internal input capacitance (6 to 10pF). No external capacitance is needed for a source resistance, R_p, less than 20KΩ. For a source resistance greater than 20KΩ, C_f = 10pF will insure stability for all gains. Maximum bandwidth may be obtained for inverting gains, R_2/R_1, greater than unity by using the relationship



$$R_p = \frac{R_1 R_2}{R_1 + R_2} \qquad C_f = \frac{10}{R_2/R_1}\,pF.$$

Section III
Voltage Regulators

104 Series

104•204•304

Negative Voltage Regulators

Features

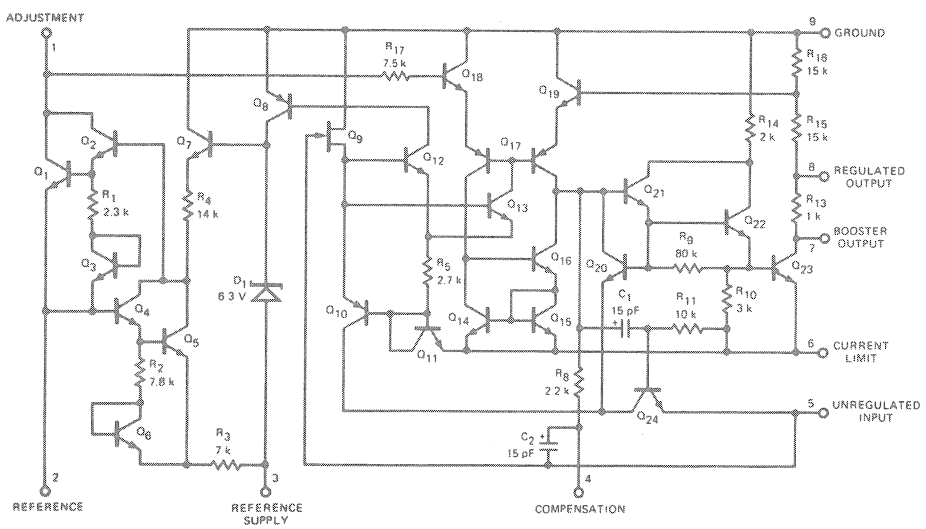
- LOAD REGULATION 1mV WITH FULL LOAD
- LINE REGULATION 0.01%/V
- RIPPLE REJECTION 0.2mV/V
- TEMPERATURE STABILITY 0.3% OVER FULL TEMPERATURE RANGE

Description

The 104, 204, 304 devices are high precision negative voltage regulators which can be programmed by a single external resistor to supply voltages from −40V to 0V while operating from a single unregulated supply. Their current capability can be boosted with the addition of an external pass transistor. When used with a separate, floating, pre-regulated bias supply it can provide better than 0.01% line regulation. External resistors are used to control the output current limiting in either constant or fold-back modes. When used in conjunction with the 105 positive voltage regulator, complementary operation can be achieved. Although designed primarily as a series regulator, the 104 can be used as a switching regulator, current regulator, or in various control applications.

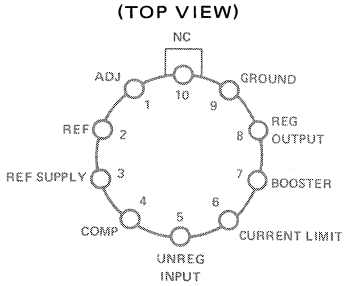
The 104 operates over the military temperature range of −55°C to +125°C. The 304 is the commercial version which operates from 0°C to +70°C. The 204 is the same as the 104 except its performance is guaranteed from −25°C to +85°C.

Equivalent Circuit Diagram



Connection Diagram

E PACKAGE
10 LEAD METAL CAN
(TOP VIEW)



Order Part Numbers:
LM104H
LM204H
LM304H

Absolute Maximum Ratings

	104	204	304
Input Voltage	50V	50V	40V
Input-Output Voltage Differential	50V	50V	40V
Power Dissipation (Note 1)	500mW	500mW	500mW
Storage Temperature Range	-65°C/+150°C	-65°C/+150°C	-65°C/+150°C
Operating Temperature Range	-55°C/+125°C	-25°C/+85°C	0°C/+70°C
Lead Temperature (Soldering, 10 sec.)	300°C	300°C	300°C
Junction Temperature	150°C	150°C	150°C

Electrical Characteristics (Note 2) 104

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Input Voltage Range			−50		−8.0	V
Output Voltage Range			−40		−0.015	V
Output/Input Voltage Differential (Note 3)	I_{OUT} = 20 mA		2.0		50	V
	I_{OUT} = 5 mA		0.5		50	V
Load Regulation (Note 4)	$0 \leq I_{OUT} \leq 20$ mA, R_{SC} = 15 Ω			1.0	5.0	mV
Line Regulation (Note 5)	$V_{OUT} \leq -5$ V, $\Delta V_{IN} = 0.1\ V_{IN}$			0.056	0.1	%
Ripple Rejection	C_{19} = 10 μF, f = 120 Hz,	$V_{IN} \geq -15$ V		0.2	0.5	mV/V
		$-7\ V \geq V_{IN} \geq -15$ V		0.5	1.0	mV/V
Output Voltage Scale Factor	R_{23} = 2.4 kΩ		1.8	2.0	2.2	V/kΩ
Temperature Stability	$V_{OUT} \leq -1$ V, −55 C ≤ $T_A \leq 125$°C			0.3	1.0	%
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, $V_{OUT} \leq -5$ V,	C_{19} = 0		0.007		%
		C_{19} = 10 μF		15		μV
Standby Current Drain	I_L = 5 mA	V_{OUT} = 0		2.1	2.5	mA
		V_{OUT} = −40 V		3.6	5.0	mA
Long Term Stability	$V_{OUT} \leq -1$ V			0.1	1.0	%

Electrical Characteristics (Note 2) 304

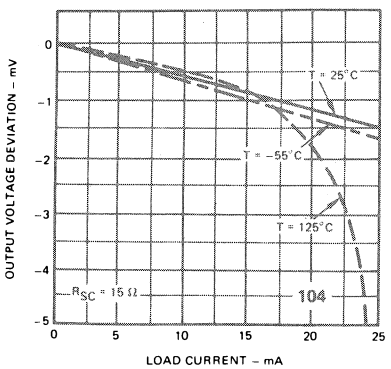
PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Input Voltage Range			−40		−8.0	V
Output Voltage Range			−30		−0.035	V
Output/Input Voltage Differential (Note 3)	I_{OUT} = 20 mA		2.0		40	V
	I_{OUT} = 5 mA		0.5		40	V
Load Regulation (Note 4)	$0 \leq I_{OUT} \leq 20$ mA, R_{SC} = 15 Ω			1.0	5.0	mV
Line Regulation (Note 5)	$V_{OUT} \leq -5$ V, $\Delta V_{IN} = 0.1\ V_{IN}$			0.056	0.1	%
Ripple Rejection	C_{19} = 10 μF, f = 120 Hz,	$V_{IN} < -15$ V		0.2	0.5	mV/V
		$-7\ V \geq V_{IN} \geq -15$ V		0.5	1.0	mV/V
Output Voltage Scale Factor	R_{23} = 2.4 kΩ		1.8	2.0	2.2	V/kΩ
Temperature Stability	$V_{OUT} \leq -1$ V, 0°C ≤ $T_A \leq 70$°C			0.3	1.0	%
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, $V_{OUT} \leq -5$ V,	C_{19} = 0		0.007		%
		C_{19} = 10 μF		15		μV
Standby Current Drain	I_L = 5 mA	V_{OUT} = 0		2.1	2.5	mA
		V_{OUT} = −30 V		3.6	5.0	mA
Long Term Stability	$V_{OUT} \leq -1$ V			0.1	1.0	%

NOTES:

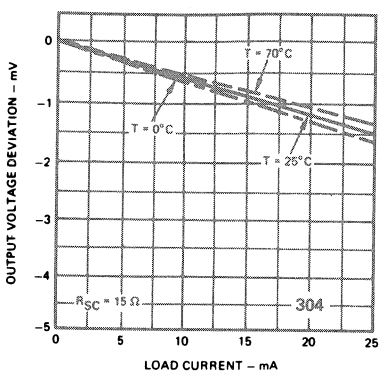
1. For operating at elevated temperatures, the device must be de-rated, based on 150°C maximum junction temperature for the 104 and 85°C for the 304 and a thermal resistance of 45°C/W junction to case or 150°C/W junction to ambient. Peak dissipations to 1.0W are allowable providing the dissipation rating is not exceeded with the power averaged over a two second interval.
2. These specifications apply for junction temperatures between −55°C and 150°C (between 0°C and 65°C for 304) and for input and output voltages within the ranges given, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.
3. When external booster transistors are used, the minimum input-output voltage differential is increased, in the worst case, by approximately one volt.
4. The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.
5. With zero output, the dc line regulation is determined from the ripple rejection. Hence, with output voltages between 0V and −5V, a DC output variation, determined from the ripple rejection, must be added to find the worst-case line regulation.

Typical Characteristics

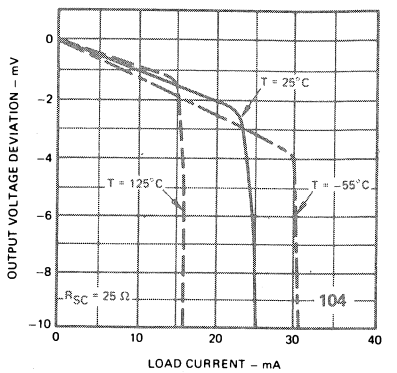
LOAD REGULATION



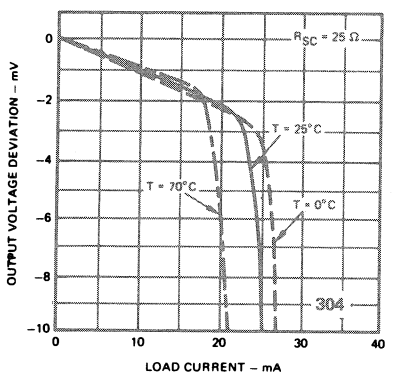
LOAD REGULATION



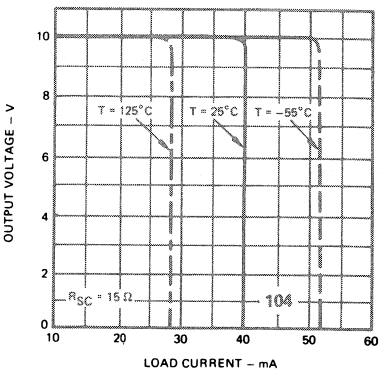
LOAD REGULATION



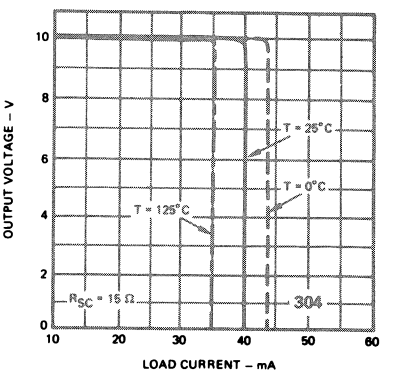
LOAD REGULATION



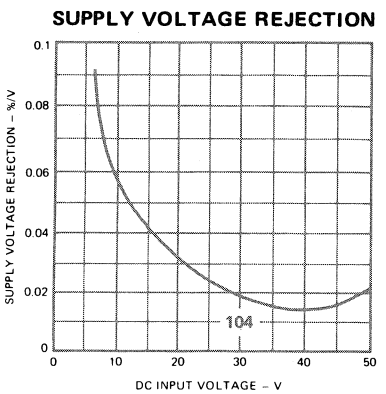
CURRENT LIMITING



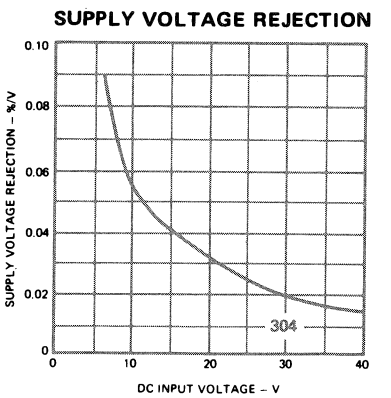
CURRENT LIMITING



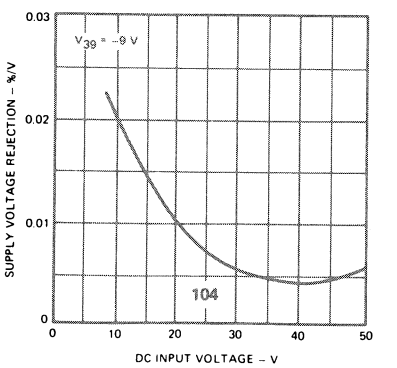
SUPPLY VOLTAGE REJECTION



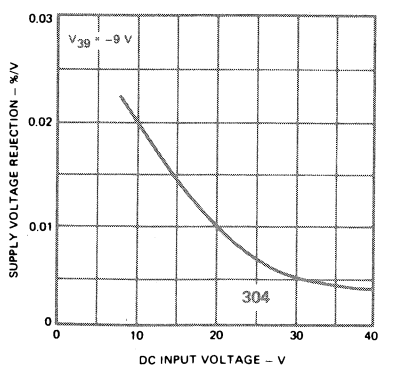
SUPPLY VOLTAGE REJECTION



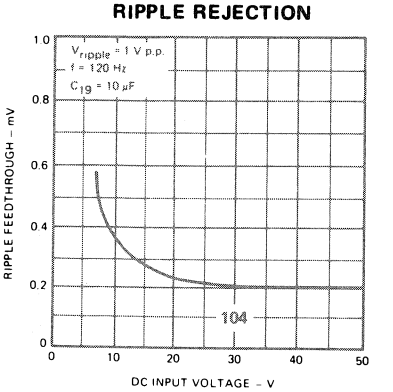
SUPPLY VOLTAGE REJECTION WITH PREREGULATED REFERENCE SUPPLY



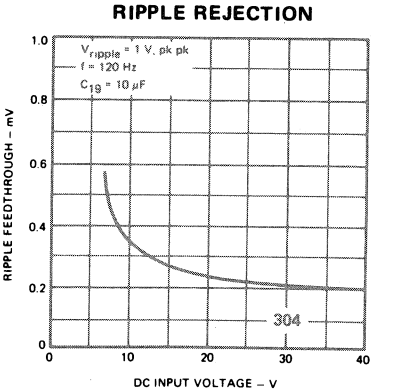
SUPPLY VOLTAGE REJECTION WITH PREREGULATED REFERENCE SUPPLY



RIPPLE REJECTION

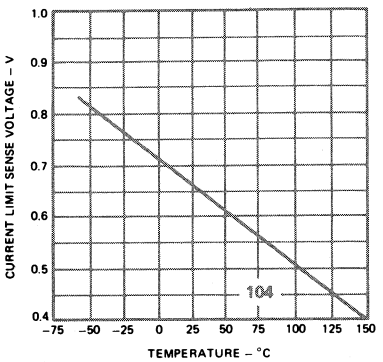


RIPPLE REJECTION

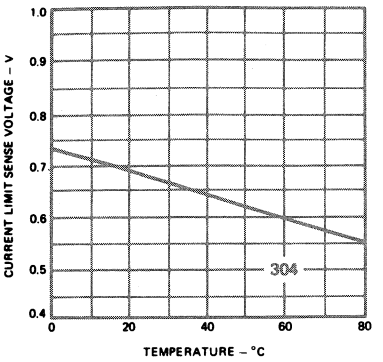


Typical Characteristics (Cont'd.)

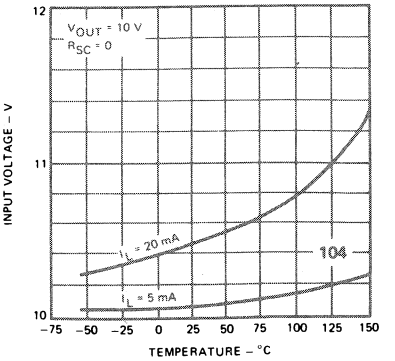
CURRENT LIMIT SENSE VOLTAGE



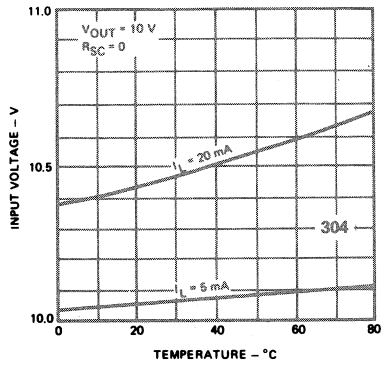
CURRENT LIMIT SENSE VOLTAGE



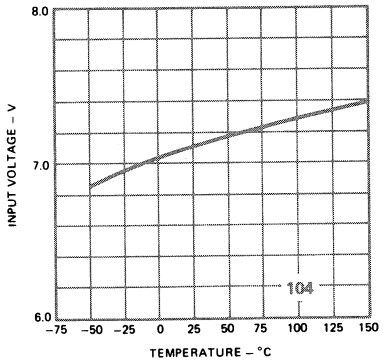
REGULATOR DROPOUT VOLTAGE



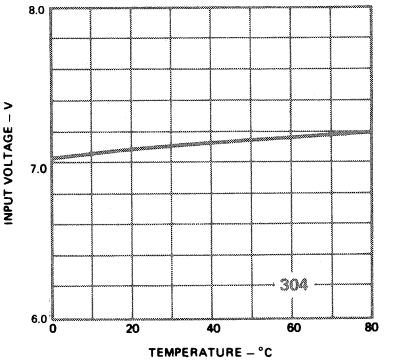
REGULATOR DROPOUT VOLTAGE



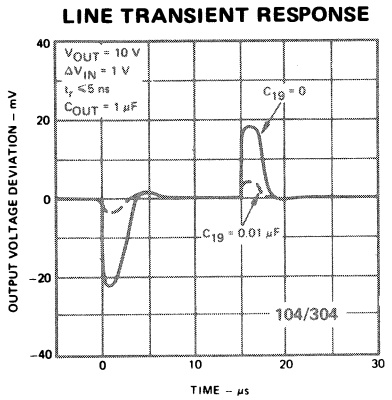
MINIMUM INPUT VOLTAGE



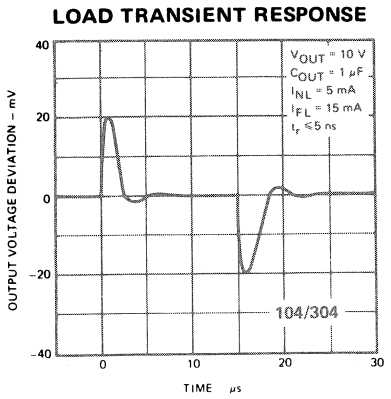
MINIMUM INPUT VOLTAGE



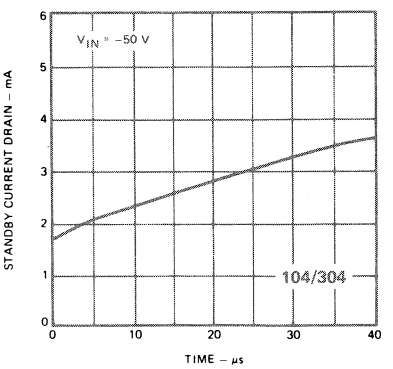
LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



STANDBY CURRENT DRAIN



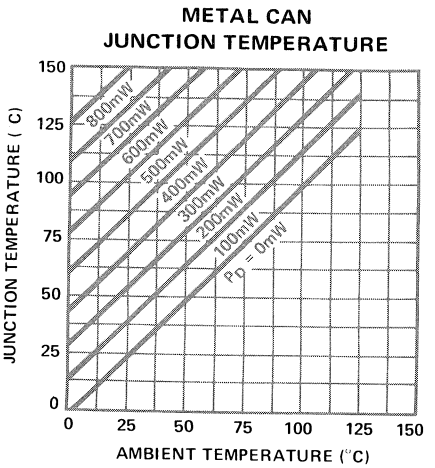
Typical Applications

Due to the wide variation of possible conditions under which these devices can be operated, it becomes difficult, if not impossible, to put worst-case limits on the device that cover more than one or two "spot" conditions. Rather than eliminate this information entirely, we have chosen to present it in the following way. In this section are a set of curves with the attendant design rules that allow them to be used for "worst case" designs.

Typical Applications (Cont'd.)

Determine the maximum allowable power dissipation, P_D. Using the highest ambient temperature in which the device is expected to operate, and the maximum junction temperature permitted (see absolute maximum ratings), and pick off the maximum allowable power dissipation.

EXAMPLE: The regulator will be called on to operate in ambient temperatures of T_A = 60°C maximum. The junction temperature has been restricted to T_J = 125°C maximum. The maximum allowable power dissipation, P_D, is 400mW.

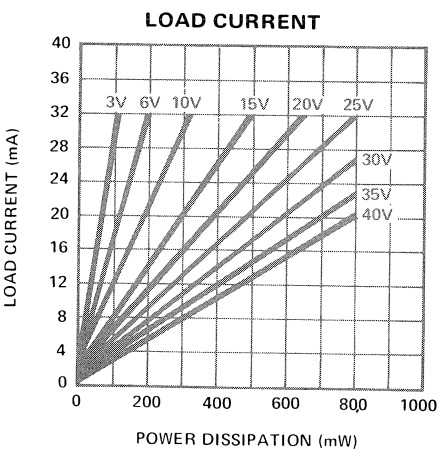


Determine the maximum allowable power dissipation due to the load current alone. This is done by subtracting the power dissipation due to standby current from P_D.

P_D (load) = P_D (total) − (V_{IN} x $I_{STANDBY}$)
EXAMPLE: V_{IN} = 25V, $I_{STANDBY}$ = 2mA (from table of electrical characteristics). P_D = 400mW ∴ P_D (load) = 400mW − (25V x 2mA) = 400 −50 = 350mW.

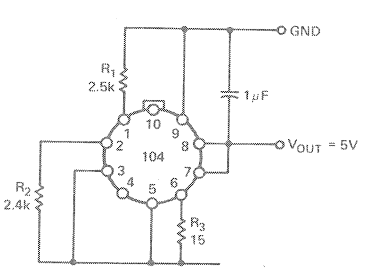
Determine the maximum IC regulator load current allowable. Note: This is the load current the 104 can deliver under your specified conditions. It is not the total load current your regulator design will be able to deliver. That is determined by external transistors that will be added. Use the P_D (load) and the V_{IN} −V_{OUT} already determined.

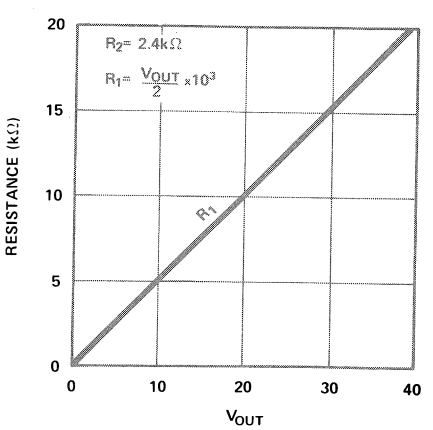
EXAMPLE: With P_D (load) = 350mW and V_{IN} −V_{OUT} = 25V the maximum load current is 14mA.



Determine the size of the programming resistor used to set the value of the output voltage.

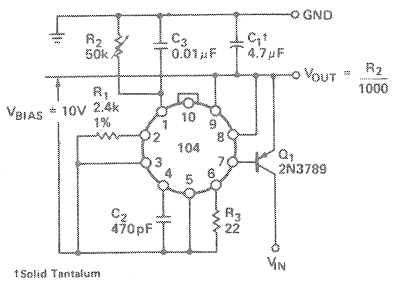
EXAMPLE: V_{OUT} = 5V ∴ R_2 = 2.4Ω and R_1 = 2.5kΩ





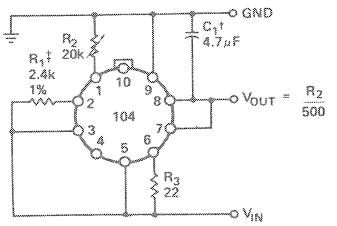
Typical Applications (Cont'd.)

OPERATING WITH SEPARATE BIAS SUPPLY



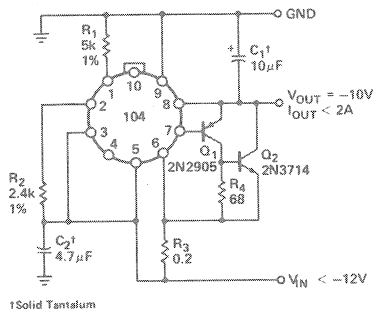
†Solid Tantalum

BASIC REGULATOR CIRCUIT



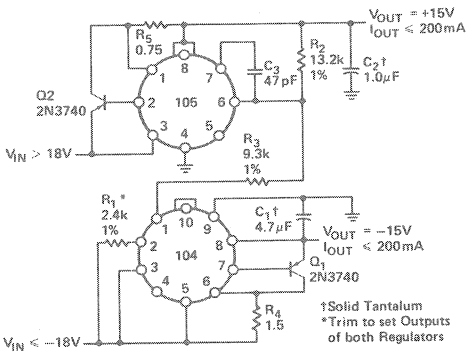
†Solid Tantalum. ‡Trim R_1 for exact scale factor.

HIGH CURRENT REGULATOR



†Solid Tantalum

SYMMETRICAL POWER SUPPLIES



†Solid Tantalum
*Trim to set Outputs of both Regulators

105 Series

105•205•305•305A

Voltage Regulators

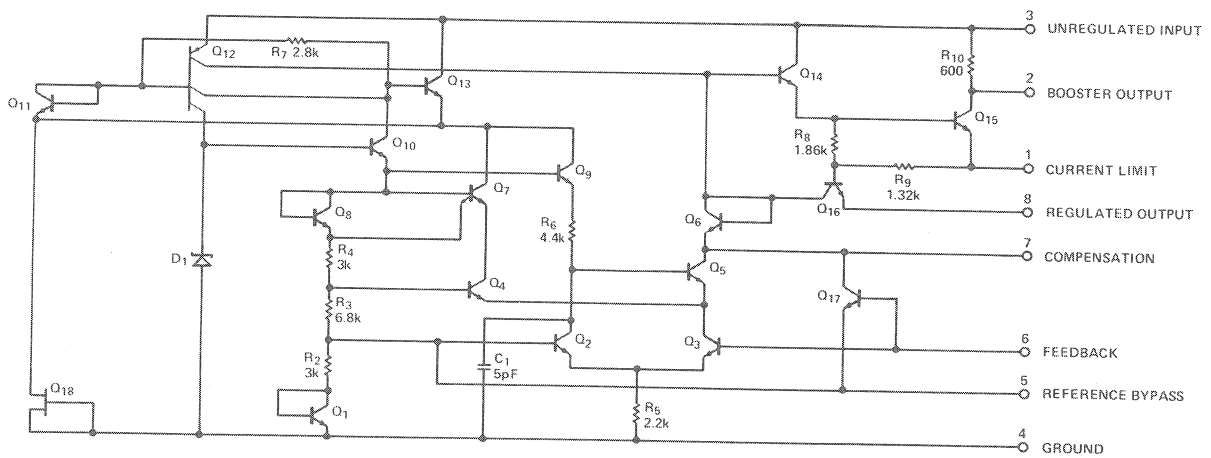
Features

- OUTPUT VOLTAGE ADJUSTABLE FROM 4.5V TO 40V
- OUTPUT CAPABILITY UP TO 10A USING EXTERNAL TRANSISTORS
- LOAD REGULATION GUARANTEED 0.1% FULL LOAD
- LINE REGULATION GUARANTEED 0.03%/V
- RIPPLE REJECTION 0.01%/V
- DESIGNERS' GUIDE SIMPLIFIES REGULATOR DESIGN

Description

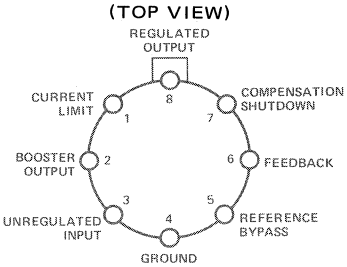
The Teledyne Semiconductor 105, 205, 305, and 305A precision voltage regulators feature a single monolithic substrate using planar epitaxial techniques. This positive voltage regulator is designed for use in linear and switching regulator circuits. External transistors can be used to increase the output current capability to greater than 10A.

Equivalent Circuit Diagram



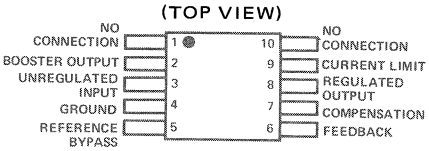
Connection Diagrams

E PACKAGE
8 LEAD METAL CAN
(TOP VIEW)



Order Part Numbers:
LM105F, LM205F

H PACKAGE
10 LEAD FLATPACK
(TOP VIEW)



Order Part Numbers:
LM105H, LM205H,
LM305H, LM305AH

Absolute Maximum Ratings

	105	205
Input Voltage	50V	50V
Input/Output Voltage Differential	40V	40V
Internal Power Dissipation (Note 1)		
Metal Can (H)	800mW	800mW
Flatpack (F)	650mW	650mW
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C	−25°C to +85°C
Lead Soldering Temperature (60 sec)	300°C	300°C
Junction Temperature	150°C	150°C
	305	**305A**
Input Voltage	40V	50V
Input/Output Voltage Differential	40V	40V
Internal Power Dissipation (Note 1)		
Metal Can (H)	800mW	800mW
Storage Temperature Range	−65°C to +85°C	−65°C to +150°C
Operating Temperature Range	0°C to +70°C	0°C to +70°C
Lead Soldering Temperature (60 sec.)	300°C	300°C
Junction Temperature	85°C	150°C

NOTES:

1. For operation at elevated temperatures, the devices must be derated by the thermal resistance method (TO5 . . . 150°C/W, junction to ambient, or 45°C/W junction to case; flatpack . . . 185°C/W when mounted on 1/16" thick epoxy glass board with ten, 0.03" wide, 2 ounce copper conductors. Peak dissipations to 1W are allowable providing the dissipation rating is not exceeded with the power averaged over a five second interval for the 105 and 205, and averaged over a 2 second interval for the 305.

Electrical Characteristics

PARAMETER	CONDITIONS	105			205			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage Range		8.5		50	8.5		50	V
Output Voltage Range		4.5		40	4.5		40	V
Input/Output Voltage Differential		3.0		30	3.0		30	V
Load Regulation (Note 3)								
105	$0 \leq I_O \leq 12mA$							
	$R_{SC} = 10\Omega$, $T_A = 25°C$		0.02	0.05				%
	$R_{SC} = 10\Omega$, $T_A = 125°C$		0.03	0.1				%
	$R_{SC} = 10\Omega$, $T_A = -55°C$		0.03	0.1				%
205	$0 \leq I_O \leq 12mA$							
	$R_{SC} = 10\Omega$, $T_A = 25°C$					0.02	0.05	%
	$R_{SC} = 10\Omega$, $T_A = 85°C$					0.03	0.1	%
	$R_{SC} = 10\Omega$, $T_A = -25°C$					0.03	0.1	%
Line Regulation	$V_{IN} - V_{OUT} \leq 5V$		0.025	0.06		0.025	0.06	%/V
	$V_{IN} - V_{OUT} > 5V$		0.015	0.06		0.015	0.03	%/V
Ripple Rejection	$C_{REF} = 10\mu F$, f = 120Hz		0.003	0.01		0.003	0.01	%/V
Temperature Stability								
105	$-55°C \leq T_A \leq 125°C$		0.3	1.0				%
205	$-25°C \leq T_A \leq 85°C$					0.3	1.0	%
Feedback Sense Voltage		1.63	1.7	1.81	1.63	1.7	1.81	V
Output Noise Voltage	$10Hz \leq f \leq 10KHz$							
	$C_{REF} = 0$		0.005			0.005		%
	$C_{REF} > 0.1\mu F$		0.002			0.002		%
Current Limit Sense Voltage	$R_{SC} = 10\Omega$, $T_A = 25°C$, $V_{OUT} = 0V$	225	300	375	225	300	375	mV
Standby Current Drain	$V_{IN} = 50V$		0.8	2.0		0.8	2.0	mA
Long Term Stability			0.1	1.0		0.1	1.0	%

Electrical Characteristics (Cont'd.)

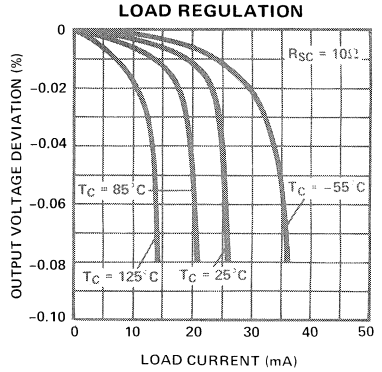
PARAMETER	CONDITIONS	305			305A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage Range		8.5		40	8.5		50	V
Output Voltage Range		4.5		30	4.5		40	V
Input/Output Voltage Differential		3.0		30	3.0		30	V
Load Regulation (Note 3) 305	$0 \leq I_O \leq 12mA$							
	$R_{SC} = 10\Omega$, $T_A = 25°C$		0.02	0.05				%
	$R_{SC} = 15\Omega$, $T_A = 70°C$		0.03	0.1				%
	$R_{SC} = 10\Omega$, $T_A = 0°C$		0.03	0.1				%
305A	$0 \leq I_O \leq 45mA$							
	$R_{SC} = 0\Omega$, $T_A = 25°C$					0.02	0.2	%
	$R_{SC} = 0\Omega$, $T_A = 70°C$					0.03	0.4	%
	$R_{SC} = 0\Omega$, $T_A = 0°C$					0.03	0.4	%
Line Regulation	$V_{IN} - V_{OUT} \leq 5V$		0.025	0.06		0.025	0.06	%/V
	$V_{IN} - V_{OUT} > 5V$		0.015	0.03		0.015	0.03	%/V
Ripple Rejection	$C_{REF} = 10\mu F$, f = 120Hz		0.003	0.01		0.003		%/V
Temperature Stability	$0°C \leq T_A \leq 70°C$		0.3	1.0		0.3	1.0	%
Feedback Sense Voltage		1.63	1.7	1.81	1.55	1.7	1.85	V
Output Noise Voltage	$10Hz \leq f \leq 10KHz$							
	$C_{REF} = 0$		0.005			0.005		%
	$C_{REF} > 0.1\mu F$		0.002			0.002		%
Current Limit Sense Voltage (305A Note 4)	$R_{SC} = 10\Omega$, $T_A = 25°C$, $V_{OUT} = 0V$	225	300	375	225	300	375	mV
Standby Current Drain	$V_{IN} = 40V$		0.8	2.0				mA
	$V_{IN} = 50V$					0.8	2.0	mA
Long Term Stability			0.1	1.0		0.1	1.0	%

NOTES:

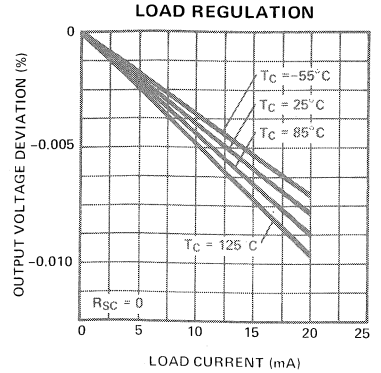
1. For operation at elevated temperatures, the devices must be derated by the thermal resistance method (TO5. . .150°C/W, junction to ambient, or 45°C/W junction to case: flatpack. . .185°C/W when mounted on 1/16" thick epoxy glass board with ten, 0.03" wide, 2 ounce copper conductors. Peak dissipations to 1W are allowable providing the dissipation rating is not exceeded with the power averaged over a five second interval for the 105 and 205, and averaged over a 2 second interval for the 305.
2. The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.
3. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.
4. (305A only) With no external pass transistor.

Typical Characteristics

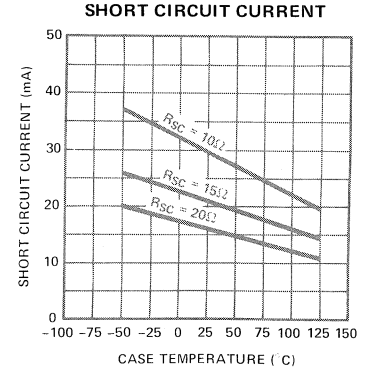
LOAD REGULATION



LOAD REGULATION

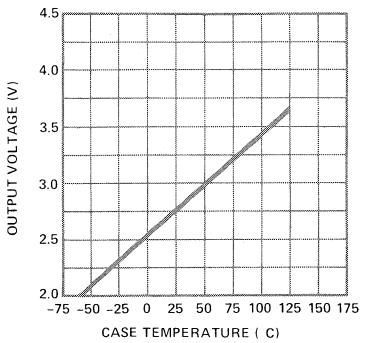


SHORT CIRCUIT CURRENT

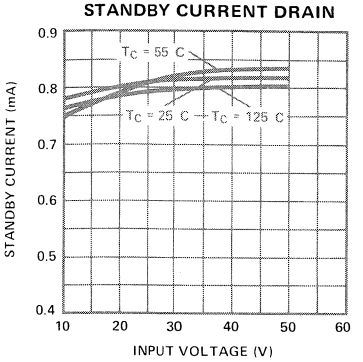


Typical Characteristics (Cont'd.)

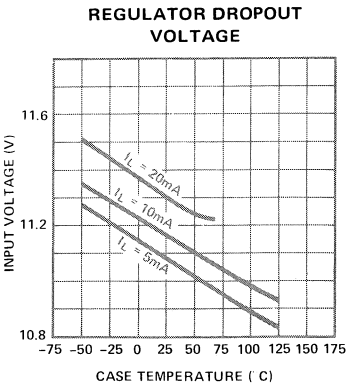
MINIMUM OUTPUT VOLTAGE



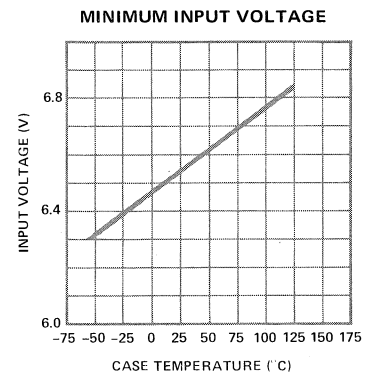
STANDBY CURRENT DRAIN



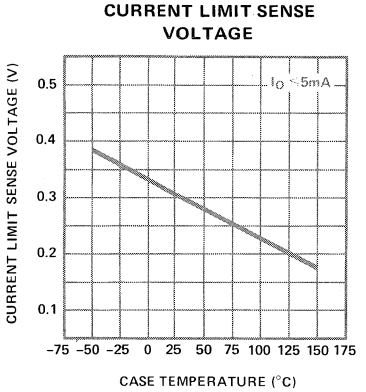
REGULATOR DROPOUT VOLTAGE



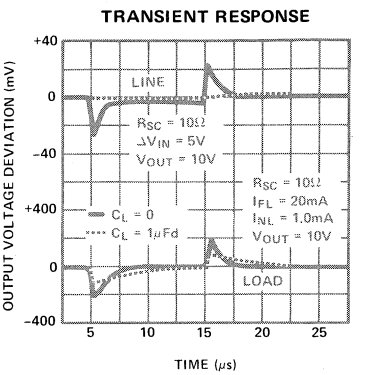
MINIMUM INPUT VOLTAGE



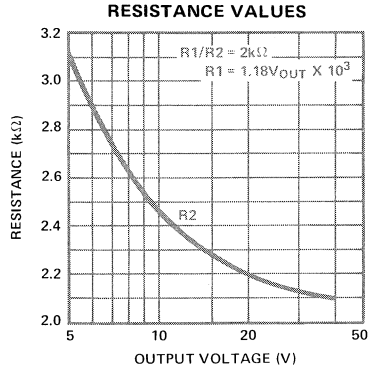
CURRENT LIMIT SENSE VOLTAGE



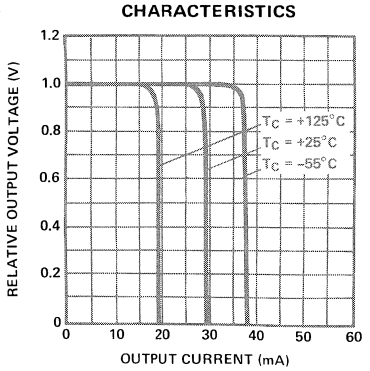
TRANSIENT RESPONSE



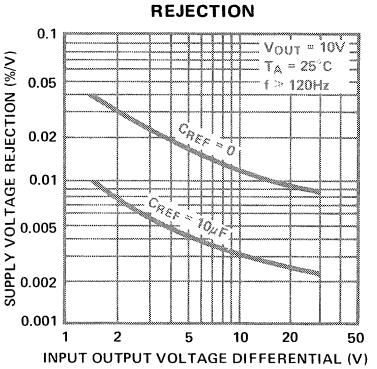
OPTIMUM DIVIDER RESISTANCE VALUES



CURRENT LIMITING CHARACTERISTICS



SUPPLY VOLTAGE REJECTION



Typical Applications

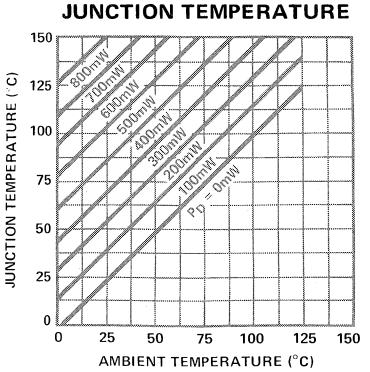
Due to the wide variation of possible conditions under which these devices can be operated, it becomes difficult if not impossible, to put worst-case limits on the device that cover more than one or two "spot" conditions. Rather than eliminate this information entirely, we have chosen to present it in the following way. In this section are a set of curves with the attendant design rules that allow them to be used for "worst-case" designs. The intention has been to present in a 1, 2, 3 fashion the basic applications information to make best use of the device.

STEP 1. Determine the maximum allowable power dissipation, P_D, from Chart 1. Use the highest ambient temperature in which the device is expected to operate, and the maximum junction temperature permitted (see absolute maximum ratings), and pick off the maximum allowable power dissipation.

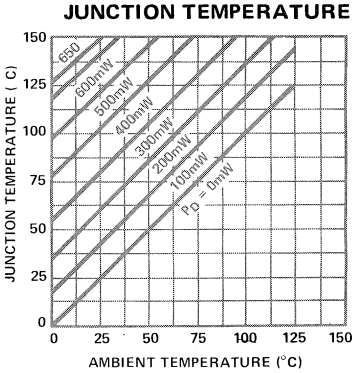
EXAMPLE: The regulator will be called on to operate in ambient temperatures of T_A = 60°C maximum. The junction temperature has been restricted to T_J = 125°C maximum. The maximum allowable power dissipation, P_D, is 400mW.

CHART 1

METAL CAN JUNCTION TEMPERATURE



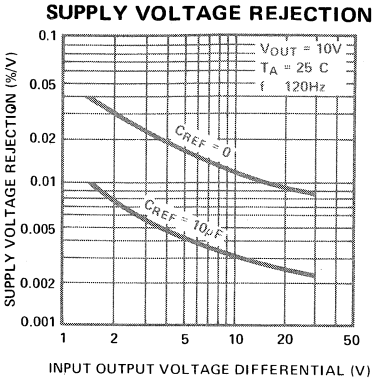
FLAT PACK JUNCTION TEMPERATURE



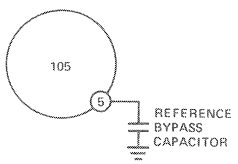
Typical Applications (Cont'd.)

STEP 2. Pick the typical line regulation your regulator should exhibit, and determine from Chart 2 the input/output voltage differential necessary to achieve this performance. This chart is also used to determine whether or not it is necessary to bypass the interval reference of the regulator with a bypass capacitor. At this point the input voltage, V_{IN}, has been determined by $V_{IN} = (V_{IN} - V_{OUT}) - V_{OUT}$.

CHART 2
SUPPLY VOLTAGE REJECTION



EXAMPLE: Desired line regulation is 0.003%/V. From Chart 2 a $V_{IN} - V_{OUT}$ of 20V should be used.

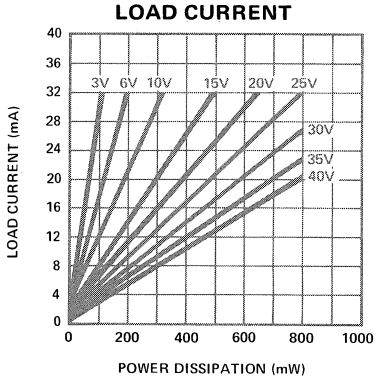


STEP 3. Determine the maximum allowable power dissipation due to the load current alone. This is done by subtracting the power dissipation due to standby current from P_D found in Step 1.

$P_D(load)_2 = P_D$ (total) $- (V_{IN} \times I_{STANDBY})$
EXAMPLE: V_{IN} = 25V, $I_{STANDBY}$ = 2mA (from table of electrical characteristics). P_D = 400mW (from Step 1). ∴ P_D (load) = 400mW – (25V x 2mA) = 400 –50 = 350mW.

STEP 4. Determine the maximum IC regulator load current allowable from Chart 3. Note: This is the load current the 105 can deliver under your specified conditions. It is not the total load current your regulator design will be able to deliver. That is determined by external transistors that will be added. Use the P_D (load) determined in Step 3 and the $V_{IN} - V_{OUT}$ determined in Step 2.

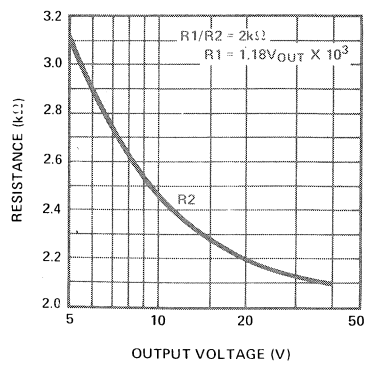
CHART 3
LOAD CURRENT



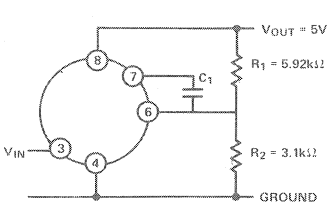
EXAMPLE: With P_D (load) = 350mW and $V_{IN} - V_{OUT}$ = 25V the max. load current, from Chart 3, is 14mA.

STEP 5. Determine the size of the two resistors used to set the value of the output voltage from Chart 4. Note: C_1 should always be 47 pF.

CHART 4
OPTIMUM DIVIDER RESISTANCE VALUES



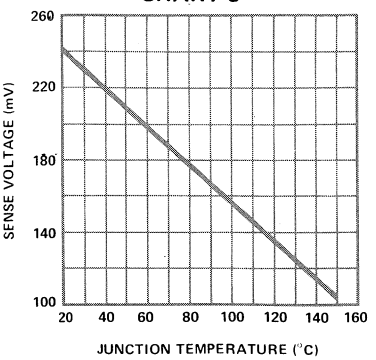
EXAMPLE: V_{OUT} = 5V ∴R_1 = 1.18 x 10^3 x 5V = 5.92kΩ. R_2 (from chart) = 3.1kΩ.



Typical Applications (Cont'd.)

STEP 6. Determine the size of the current limiting resistor from Chart 5. (This method does not work when foldback current limiting is used). Use the maximum junction temperature that was used in Step 1 to find the sense voltage that will initiate current limiting. Calculate the value of the current limiting resistor from the formula, $R_{SC} = V_{SENSE} / I_{LOAD}$, where I_{LOAD} is the maximum regulated output current of the regulator design.

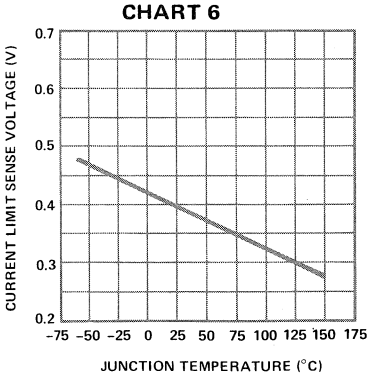
CHART 5



EXAMPLE: For a regulator designed with a max. design junction temperature of $T_J = 125°C$ and a 200 mA I_{load} output current, from Chart 5:
$R_{SC} = 130mV/200mA = 0.65\Omega$.

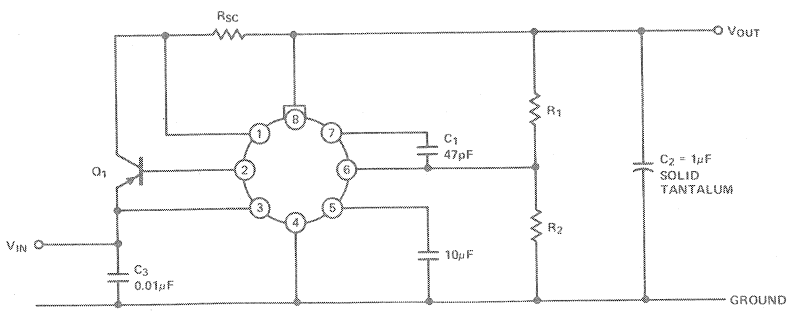
STEP 7. Determine the value of I_{SC}, output current with output shorted to ground, from Chart 6. For the maximum junction temperature, find the short circuit sense voltage, V_{SC} sense. Then calculate the value of I_{SC} from $I_{SC} = V_{SC\ SENSE} / R_{SC}$.

CHART 6



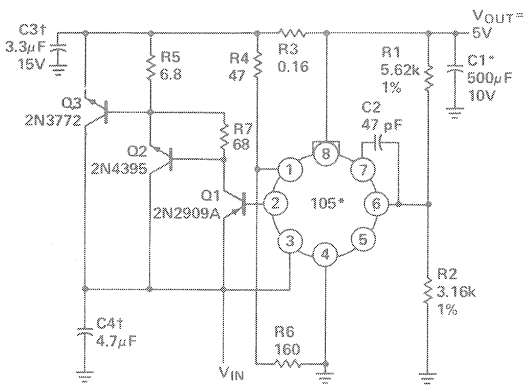
EXAMPLE: For a regulator designed with a max. junction temperature of $T_J = 125°C$, then from Chart 6, $V_{SC\ SENSE} = 0.3V$ and $I_{SC} = 0.3V/0.65\Omega$ from Step 6, $I_{SC} = 460mA$.

STEP 8. Select external pass transistor Q_1. Use I_{load} found in Step 4 for the base drive to the transistor, which must be able to pass the max. load current for the regulator with the minimum data sheet h_{FE} for Q_1. The device must dissipate steady state P_D where $P_D = (V_{IN} - V_{OUT})(I_{load})$ Step 6. If the design is to be short-circuit protected, the transistor-sink combination must be able to withstand $P_D = (V_{IN})(I_{SC})$ for the appropriate length of time. In the event that a device meeting these requirements cannot be found, it may be necessary to go to a foldback current limiting configuration.



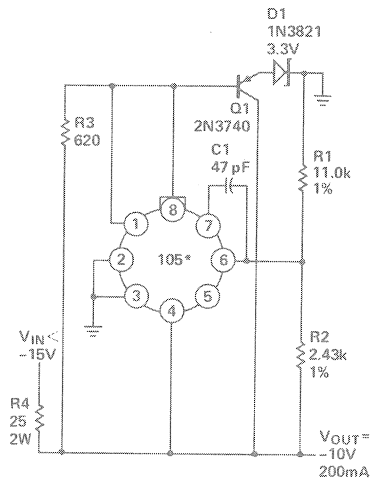
Typical Applications (Cont'd.)

10A REGULATOR WITH FOLDBACK CURRENT LIMITING

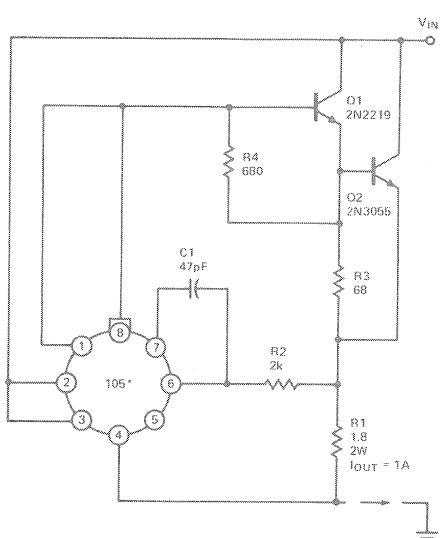


†Solid Tantalum
*Electrolytic

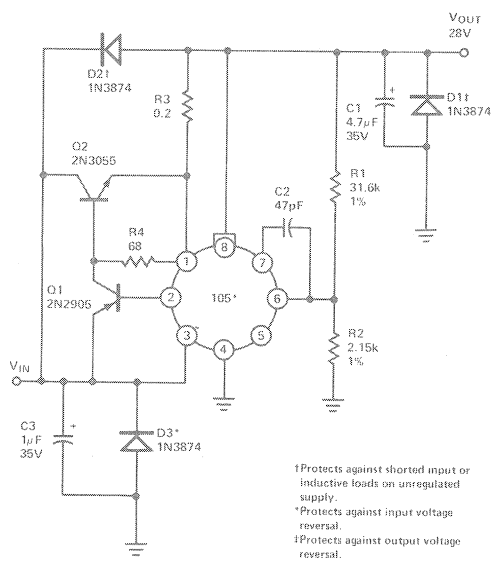
SHUNT REGULATOR



CURRENT REGULATOR

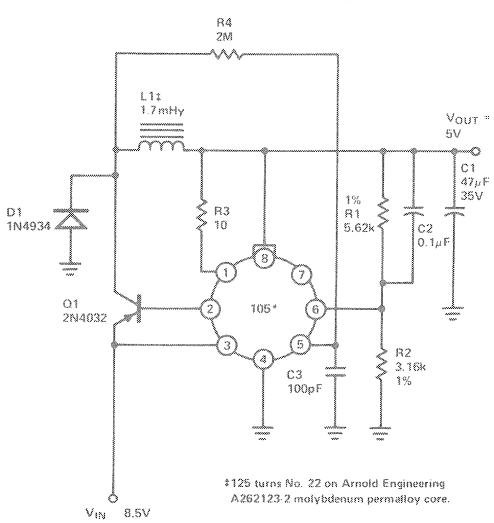


1.0A REGULATOR WITH PROTECTIVE DIODES



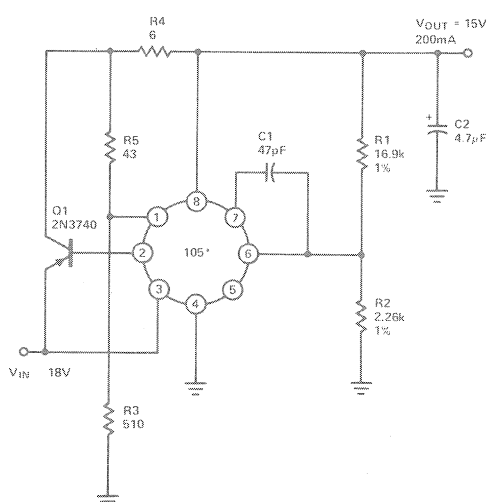
†Protects against shorted input or inductive loads on unregulated supply.
*Protects against input voltage reversal.
‡Protects against output voltage reversal.

SWITCHING REGULATOR



‡125 turns No. 22 on Arnold Engineering A262123-2 molybdenum permalloy core.

LINEAR REGULATOR WITH FOLDBACK CURRENT LIMITING



376
Voltage Regulators

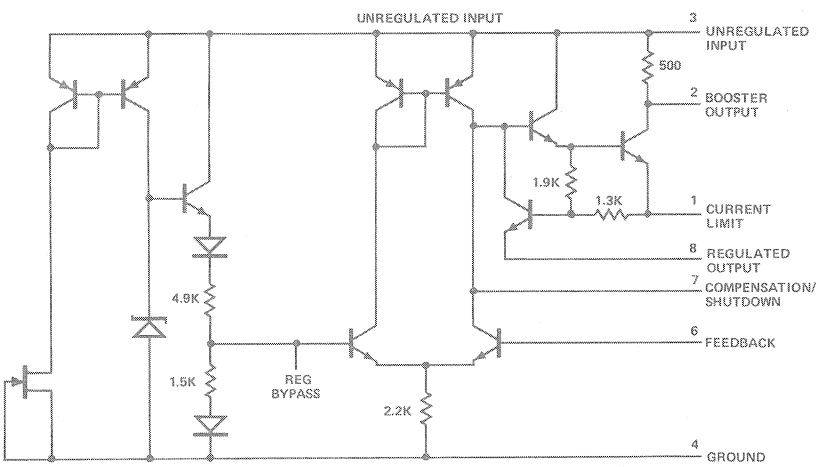
Features

- OUTPUT VOLTAGE +5 TO 37V
- OUTPUT CURRENT 25mA
- LOAD REGULATION 0.2%
- LINE REGULATION 0.03%/V
- LOW STANDBY CURRENT DRAIN

Description

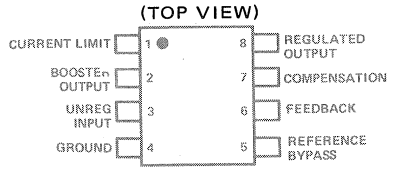
The Teledyne Semiconductor 376 is a positive voltage regulator designed primarily for commercial product applications. The device is especially useful because it is packaged in an 8-pin MINIDIP for reduced size and low cost. Used independently, the device will supply 25mA; with the addition of external pass elements, any desired load current can be achieved. The circuit features extremely low standby current drain, and provision is made for either linear or foldback current limiting.

Equivalent Circuit Diagram



Connection Diagram

P PACKAGE
8 LEAD MINIDIP
(TOP VIEW)



Order Part Number:
LM376N

Absolute Maximum Ratings

Input Voltage	40V
Input-Output Voltage Differential	40V
Power Dissipation (Note 1)	400mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

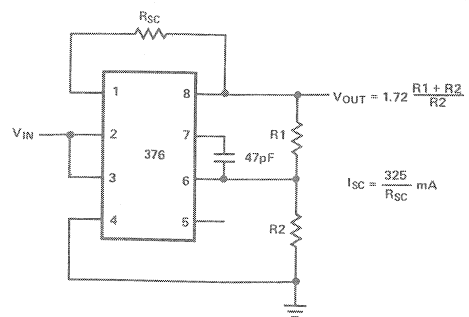
Electrical Characteristics

PARAMETER	CONDITIONS	376			UNITS
		MIN	TYP	MAX	
Input Voltage Range		9.0		40	V
Output Voltage Range		5.0		37	V
Input/Output Voltage Differential		3.0		30	V
Load Regulation	$0 \leqslant I_O \leqslant 25mA$				
	$R_{SC} = 0\Omega$, $T_A = 25°C$			0.2	%
	$R_{SC} = 0\Omega$, $T_A = 70°C$			0.5	%
	$R_{SC} = 0\Omega$, $T_A = 0°C$			0.5	%
Line Regulation	$T_A = 25°C$			0.3	%/V
				.1	%/V
Ripple Rejection	f = 120Hz, $T_A = 25°C$			0.1	%/V
Standby Current Drain	$V_{IN} = 30V$, $T_A = 25°C$			2.5	mA
Reference Voltage		1.60	1.72	1.80	V
Current Limit Sense Voltage			.360		V

NOTES: 1. For operating at elevated temperatures, the device must be derated based on a 100°C maximum junction temperature and a thermal resistance of 187°C/W junction to ambient.
2. These specifications apply for an operating temperature between 0°C and 70°C.

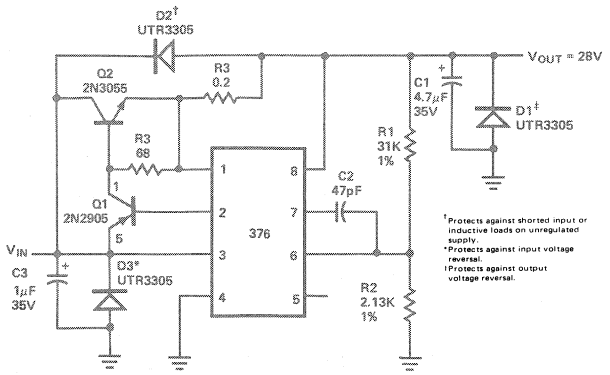
Typical Applications

BASIC POSITIVE REGULATOR WITH CURRENT LIMITING

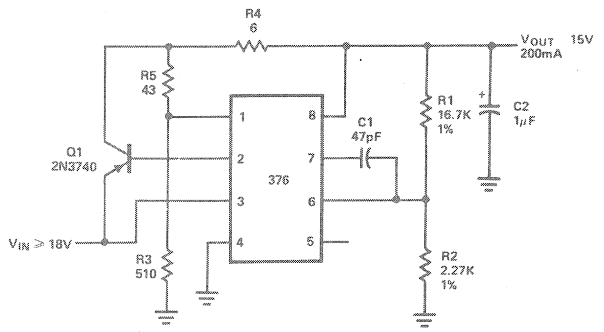


Typical Applications (Cont'd.)

1.0A REGULATOR WITH PROTECTIVE DIODES



LINEAR REGULATOR WITH FOLDBACK CURRENT LIMITING



723
Voltage Regulators

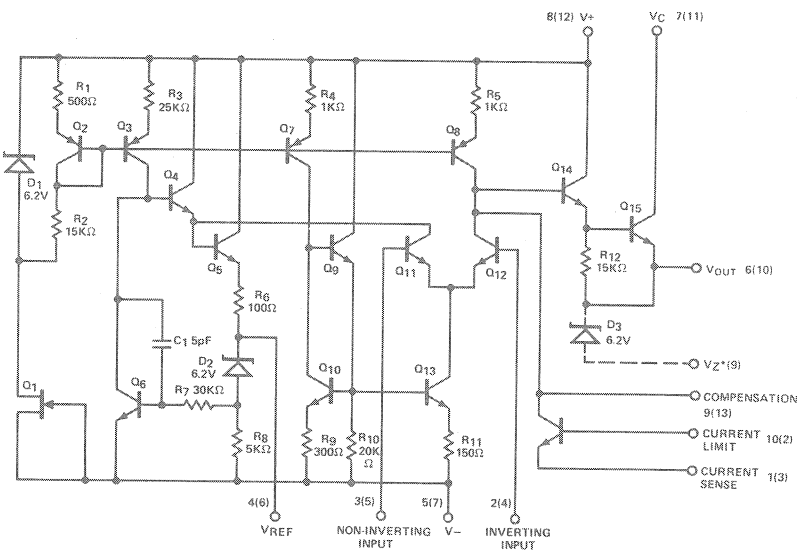
Features

- POSITIVE OR NEGATIVE SUPPLY OPERATION
- SERIES, SHUNT, SWITCHING OR FLOATING APPLICATIONS
- HIGH PERFORMANCE LINE AND LOAD REGULATION – .01%
- LOW OUTPUT VOLTAGE DRIFT – .002%/°C TYP
- BASIC OUTPUT CURRENT 150mA – BOOSTABLE
- ADJUSTABLE OUTPUT VOLTAGE – 2 TO 37 VOLTS

Description

The Teledyne Semiconductor 723 is a monolithic voltage regulator constructed using planar epitaxial techniques. The device consists of several basic regulator building blocks of temperature compensated reference and buffer amplifier, error amplifier, power series pass transistor, and current limiting circuitry. This device features extremely low output voltage drift with temperature and is ideally suited as a positive or negative regulator in series, shunt, switching, or floating applications. The output current capability of the 723 is 150mA which can be boosted by the addition of external PNP or NPN pass elements.

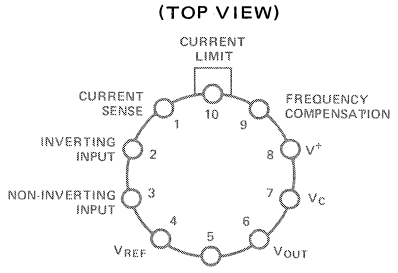
Equivalent Circuit Diagram



L Package pinouts in parentheses.
*V_Z connection is only available in "dual-in-line package".

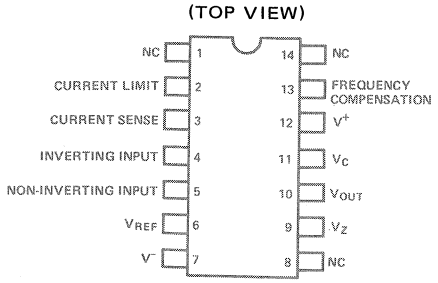
Connection Diagrams

E PACKAGE
10 LEAD METAL CAN
(TOP VIEW)



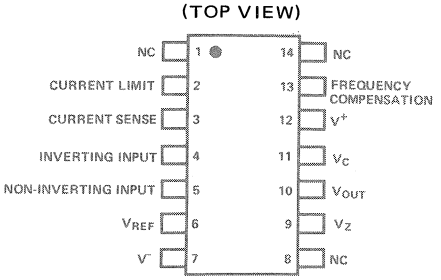
Order Part Numbers:
723BE, 723CE

L PACKAGE
14 LEAD CERDIP
(TOP VIEW)



Order Part Numbers:
723BL, 723CL

J PACKAGE
14 LEAD PLASTIC DIP
(TOP VIEW)



Order Part Number:
723CJ

Absolute Maximum Ratings

		723	723C
Input/Output Voltage Differential		40V	40V
Maximum Output Current		150mA	150mA
Pulse Voltage from V^+ to V^- (50 msec)		50V	40V
Continuous Voltage from V^+ to V^-		40V	40V
Current from V_{REF}		15mA	15mA
Current from V_Z		25mA	25mA
Internal Power Dissipation (Note 1)	"E" Package	800mW	800mW
	TO-116 "L" Package	900mW	900mW
	TO-116 "J" Package	NA	780mW
Storage Temperature Range		−65°C/+150°C	−65°C/+150°C
Operating Temperature Range		−55°C/+125°C	0°C/+70°C
Lead Temperature (Soldering, 60 sec)		300°C	300°C

Electrical Characteristics

at T_A = 25°C, $V_{IN} = V^+ = V_C$ = 12V, V^- = 0, V_{OUT} = 5V, I_L = 1 mA, R_{SC} = 0, C_1 = 100 pF, C_{REF} = 0 and divider impedance as seen by error amplifier ≤ 10 KΩ connected as shown in Figure 1 (Unless Otherwise Specified)

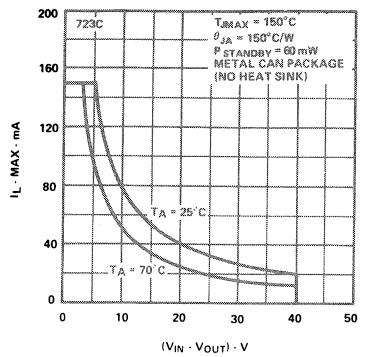
Parameter	Conditions	723			723C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Line Regulation (Note 7)	V_{IN} = 12V to V_{IN} = 15V		0.01	0.1		0.01	0.1	$\%V_{OUT}$
	V_{IN} = 12V to V_{IN} = 40V		0.02	0.2		0.1	0.5	$\%V_{OUT}$
	−55°C ≤ T_A ≤ +125°C, V_{IN} = 12V to V_{IN} = 15V			0.3				$\%V_{OUT}$
	0°C ≤ T_A ≤ 70°C, V_{IN} = 12V to V_{IN} = 15V						0.3	$\%V_{OUT}$
Load Regulation (Note 7)	I_L = 1 mA to I_L = 50 mA		0.03	0.15		0.03	0.2	$\%V_{OUT}$
	−55°C ≤ T_A ≤ +125°C, I_L = 1 mA to I_L = 50 mA			0.6				$\%V_{OUT}$
	0°C ≤ T_A ≤ 70°C, I_L = 1 mA to I_L = 50 mA						0.6	$\%V_{OUT}$
Ripple Rejection	f = 50 Hz to 10 kHz, C_{REF} = 0		74			74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF		86			86		dB
Average Temperature	−55°C ≤ T_A ≤ +125°C		0.002	0.015				%/°C
Coefficient of Output Voltage	0°C ≤ T_A ≤ 70°C					0.003	0.015	%/°C
Short Circuit Current Limit	R_{SC} = 10Ω, V_{OUT} = 0		65			65		mA
Reference Voltage		6.95	7.15	7.35	6.80	7.15	7.50	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		20			20		μV_{rms}
	BW = 100 Hz to 10 kHz, C_{REF} = 5 μF		2.5			2.5		μV_{rms}
Long Term Stability			0.1			0.1		%/1000 hrs
Standby Current Drain	I_L = 0, V_{IN} = 30V		2.3	3.5		2.3	4.0	mA
Input Voltage Range		9.5		40	9.5		40	V
Output Voltage Range		2.0		37	2.0		37	V
Input-Output Voltage Differential		3.0		38	3.0		38	V

NOTES:

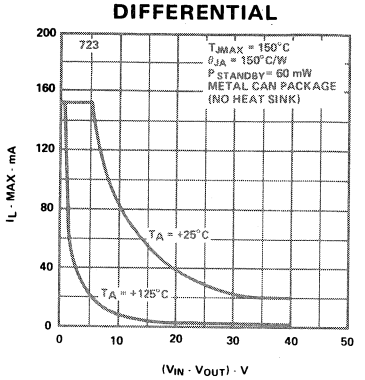
1. Derate linearly at 6.8mW/°C for metal can package, 9mW/°C for Ceramic Dual-In-Line package, and 6.3mW/°C for plastic Dual-In-Line package for operation at ambient temperatures above 25°C.
2. L_1 is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009" air gap.
3. Figures in parentheses may be used if R1/R2 divider is placed on opposite side of error amp.
4. Replace R1/R2 in figures with divider shown in Figure 13.
5. V^+ must be connected to a +3V or greater supply.
6. For metal can applications where V_Z is required, an external 6.2 volt zener should be connected in series with V_{OUT}.
7. Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken account separately for high power dissipation.

Typical Performance

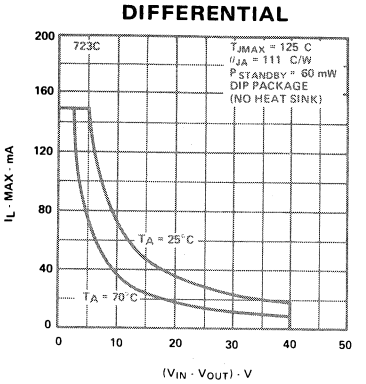
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



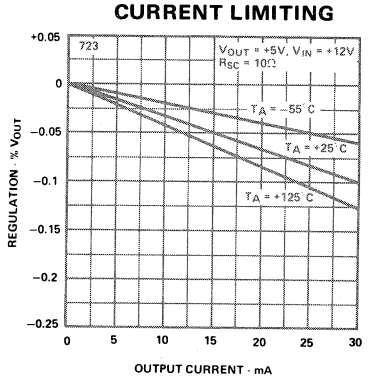
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



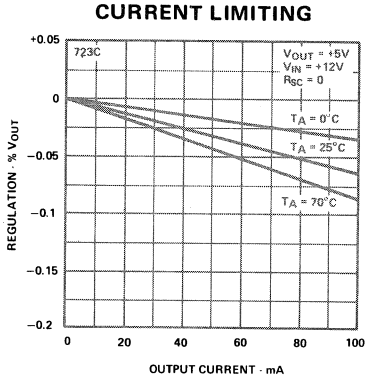
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



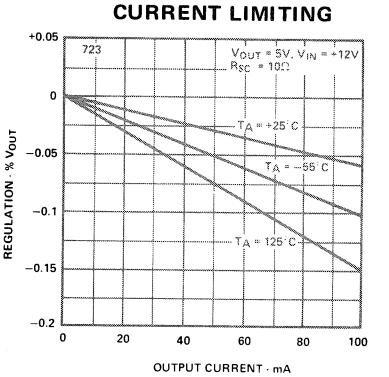
DYNAMIC LOAD CHARACTERISTICS WITH CURRENT LIMITING



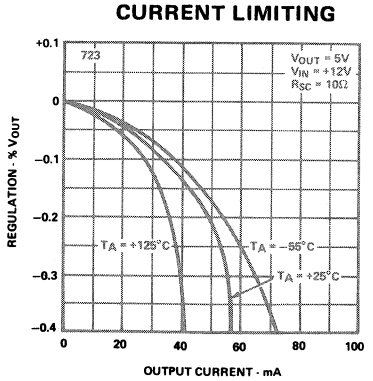
DYNAMIC LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



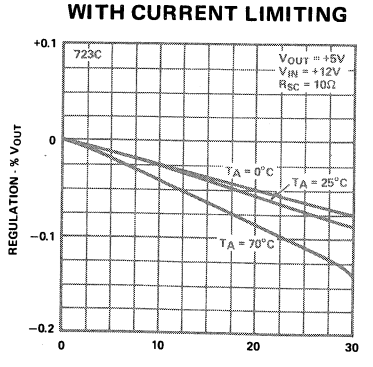
DYNAMIC LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



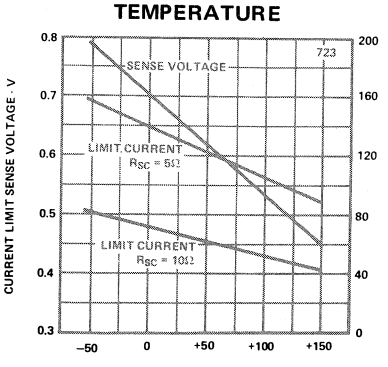
DYNAMIC LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



DYNAMIC LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

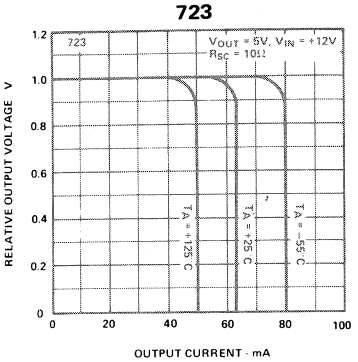


CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE

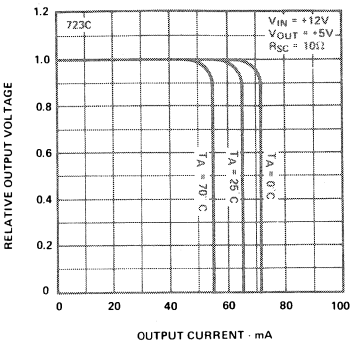


Typical Performance (cont'd.)

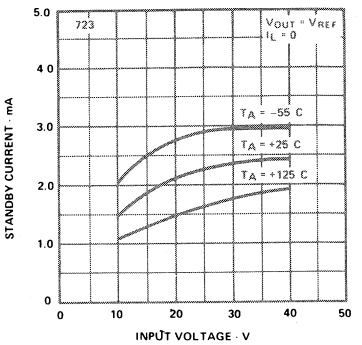
CURRENT LIMITING CHARACTERISTICS 723



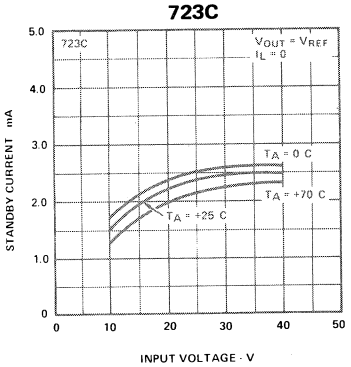
CURRENT LIMITING CHARACTERISTICS 723C



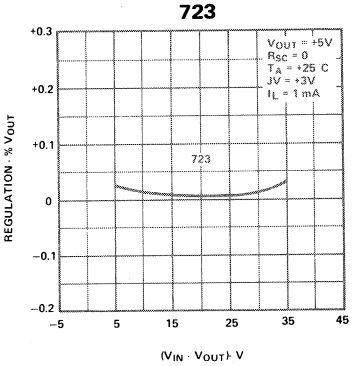
STANDBY CURRENT DRAIN VS. INPUT VOLTAGE 723



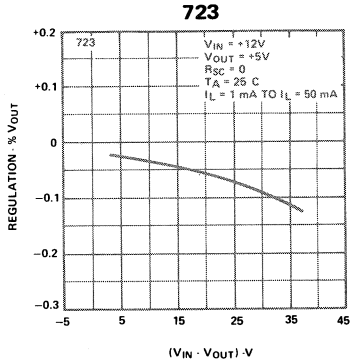
STANDBY CURRENT DRAIN VS. INPUT VOLTAGE 723C



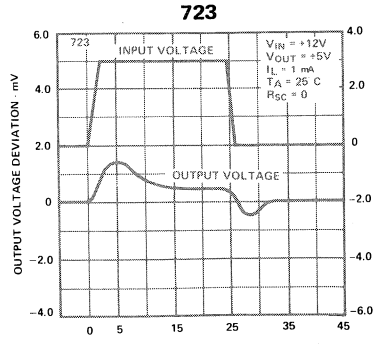
LINE REGULATION VS. INPUT-OUTPUT VOLTAGE DIFFERENTIAL 723



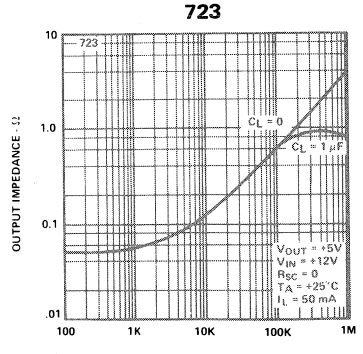
DYNAMIC LOAD REGULATION VS. INPUT-OUTPUT VOLTAGE DIFFERENTIAL 723



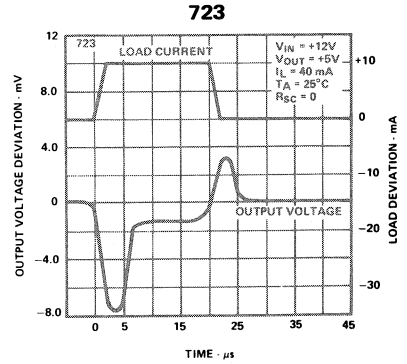
LINE TRANSIENT RESPONSE 723



OUTPUT IMPEDANCE VS. FREQUENCY 723



LOAD TRANSIENT RESPONSE 723



Typical Applications

TABLE I RESISTOR VALUES (kΩ) FOR STANDARD OUTPUT VOLTAGES

Positive Output Voltage	Applicable Figures	Fixed Output ±5%		Output Adjustable ±10% (Note 4)		
	(Note 3)	R_1	R_2	R_1	P_1	R_2
+3.0	1,5,6,9, 12(4)	4.12	3.01	1.8	0.5	1.2
+3.6	1,5,6,9, 12(4)	3.57	3.65	1.5	0.5	1.5
+5.0	1,5,6,9, 12(4)	2.15	4.99	0.75	0.5	2.2
+6.0	1,5,6,9, 12(4)	1.15	6.04	0.5	0.5	2.7
+9.0	2,4,(5,6, 12,9)	1.87	7.15	0.75	1.0	2.7
+12	2,4,(5,6, 9,12)	4.87	7.15	2.0	1.0	3.0
+15	2,4,(5,6, 9,12)	7.87	7.15	3.3	1.0	3.0
+28	2,4,(5,6, 9,12)	21.0	7.15	5.6	1.0	2.0
+45	7	3.57	48.7	2.2	10	39
+75	7	3.57	78.7	2.2	10	68

Negative Output Voltage	Applicable Figures	Fixed Output ±5%		5% Output Adjustable ±10%		
	(Note 3)	R_1	R_2	R_1	P_1	R_2
+100	7	3.57	102	2.2	10	91
+250	7	3.57	255	2.2	10	240
−6 (Note 5)	3,(10)	3.57	2.43	1.2	0.5	0.75
−9	3,10	3.48	5.36	5.36	0.5	2.0
−12	3,10	3.57	8.45	8.45	0.5	3.3
−15	3,10	3.65	11.5	1.2	0.5	4.3
−28	3,10	3.57	24.3	1.2	0.5	10
−45	8	3.57	41.2	2.2	10	33
−100	8	3.57	97.6	2.2	10	91
−250	8	3.57	249	2.2	10	240

TABLE II FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts
[Figures 1, 5, 6, 9, 12, (4)]

$$V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$$

Outputs from +7 to +37 volts
[Figures 2, 4, (5, 6, 9, 12)]

$$V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$$

Outputs from +4 to +250 volts
[Figure 7]

$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_2 + R_1}{R_1}] \; R_3 = R_4$$

Outputs from −6 to −250 volts
[Figures 3, 8, 10]

$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}] \; R_3 = R_4$$

Current Limiting

$$I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}}$$

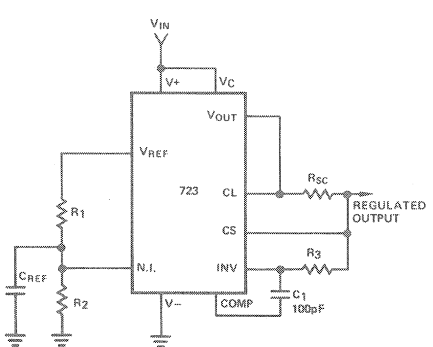
Foldback Current Limiting

$$I_{KNEE} = [\frac{V_{OUT} R_3}{R_{SC} R_4} \times \frac{V_{SENSE} (R_3 + R_4)}{R_{SC} R_4}]$$

$$I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{SC}} \times \frac{R_3 + R_4}{R_4}]$$

NOTE: Line and Load Regulation in Figures 1 through 12 are shown in mV for the convenience of the experimenter in relating to his actual meter readings.

Figure 1
BASIC LOW VOLTAGE REGULATOR
(V_{OUT} = 2 to 7 Volts)

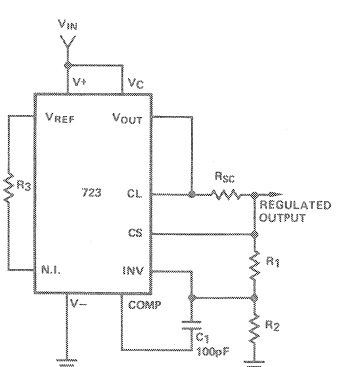


Note: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.

TYPICAL PERFORMANCE

Regulated Output Voltage	5 V
Line Regulation (ΔVin = 3V)	0.5 mV
Load Regulation (ΔI_L = 50 mA)	1.5 mV

Figure 2
BASIC HIGH VOLTAGE REGULATOR
(V_{OUT} = 7 to 37 Volts)



Note: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.

R_3 may be eliminated for minimum component count.

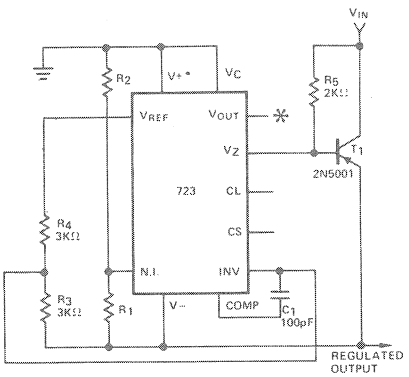
TYPICAL PERFORMANCE

Regulated Output Voltage	15 V
Line Regulation (ΔVin = 3 V)	1.5 mV
Load Regulation (ΔI_L = 50 mA)	4.5 mV

Typical Applications (cont'd.)

Figure 3

NEGATIVE VOLTAGE REGULATOR



TYPICAL PERFORMANCE

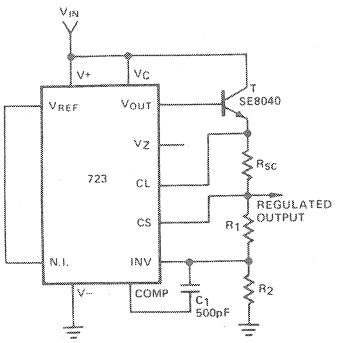
Regulated Output Voltage	−15 V
Line Regulation (Δin = 3 V)	1 mV
Load Regulation (ΔI_L = 100 mA)	2 mV

*Note 6

Figure 4

POSITIVE VOLTAGE REGULATOR

(External NPN Pass Transistor)



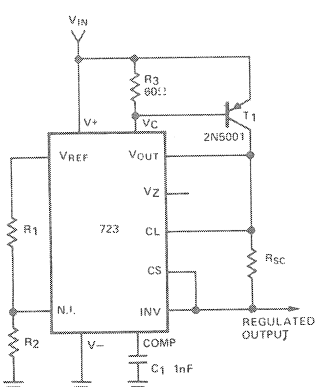
TYPICAL PERFORMANCE

Regulated Output Voltage	+15 V
Line Regulation (ΔVin = 3 V)	1.5 mV
Load Regulation (ΔI_L = 1 A)	15 mV

Figure 5

POSITIVE VOLTAGE REGULATOR

(External PNP Pass Transistor)

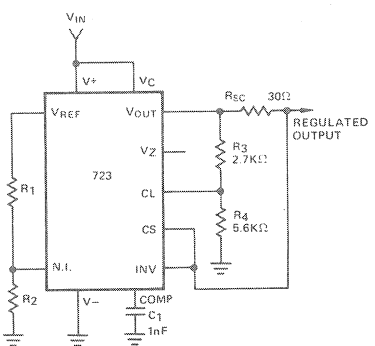


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔVin = 3 V)	0.5 mV
Load Regulation (ΔI_L = 1 A)	5 mV

Figure 6

FOLDBACK CURRENT LIMITING

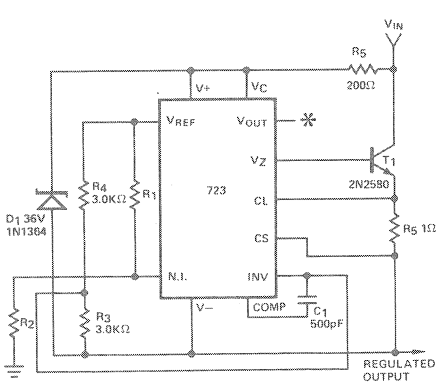


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔVin = 3 V)	0.5 mV
Load Regulation (ΔI_L = 10 mA)	1 mV
Current Limit Knee	110 mA
Short Circuit Current	20 mA

Figure 7

POSITIVE FLOATING REGULATOR



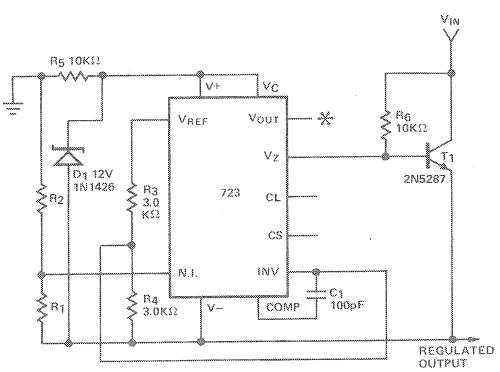
TYPICAL PERFORMANCE

Regulated Output Voltage	+50 V
Line Regulation (ΔVin = 20 V)	15 mV
Load Regulation (ΔI_L = 50 mA)	20 mV

*Note 6

Figure 8

NEGATIVE FLOATING REGULATOR



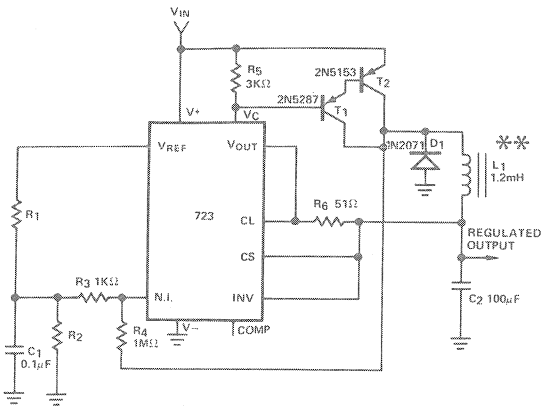
TYPICAL PERFORMANCE

Regulated Output Voltage	−100 V
Line Regulation (ΔVin = 20 V)	30 mV
Load Regulation (ΔI_L = 100 mA)	20 mV

*Note 6

Typical Applications (cont'd.)

Figure 9
POSITIVE SWITCHING REGULATOR

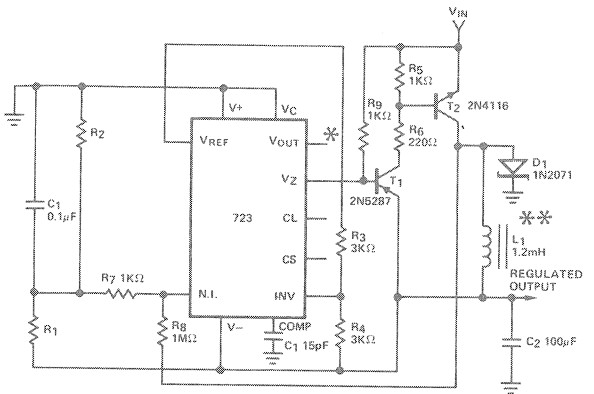


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔVin = 30 V)	10 mV
Load Regulation (ΔI_L = 2 A)	80 mV

**Note 2

Figure 10
NEGATIVE SWITCHING REGULATOR

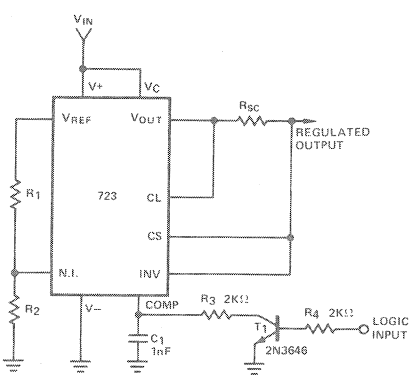


TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation (ΔVin = 20 V)	8 mV
Load Regulation (ΔI_L = 2 A)	6 mV

*Note 6 **Note 2

Figure 11
REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING



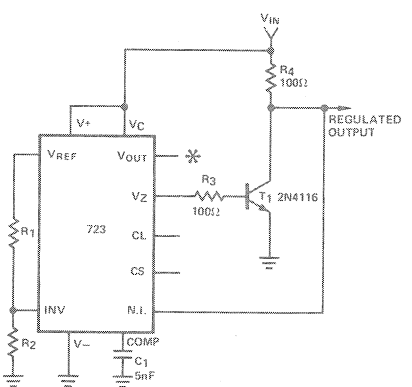
Note: Current limit transistor may be used for shutdown if current limiting is not required.

TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔVin = 3 V)	0.5 mV
Load Regulation (ΔI_L = 50 mA)	1.5 mV

*Note 6

Figure 12
SHUNT REGULATOR



TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔVin = 10 V)	0.5 mV
Load Regulation (ΔI_L = 100 mA)	1.5 mV

Figure 13
OUTPUT VOLTAGE ADJUST

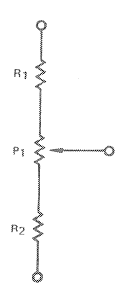
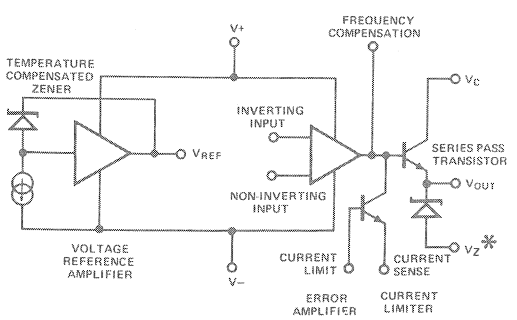


Figure 14
EQUIVALENT CIRCUIT



* V_Z connection is only available in "dual" in-line package."

823
Voltage Regulators

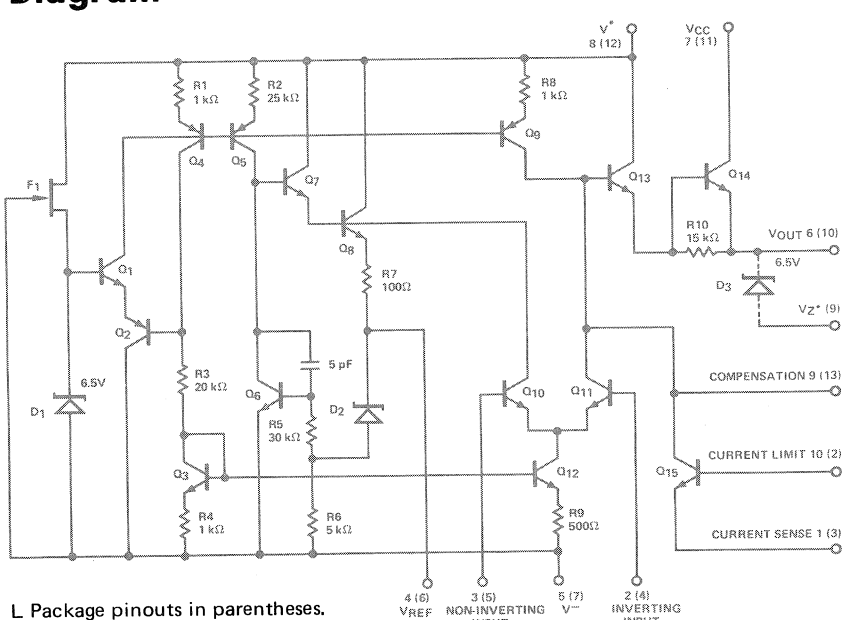
Features

- POSITIVE OR NEGATIVE SUPPLY OPERATION
- SERIES, SHUNT, SWITCHING OR FLOATING APPLICATIONS
- HIGH PERFORMANCE LINE AND LOAD REGULATION – .01%
- LOW OUTPUT VOLTAGE DRIFT – .002%/°C TYP.
- BASIC OUTPUT CURRENT 150mA – BOOSTABLE
- ADJUSTABLE OUTPUT VOLTAGE – 2 TO 37 VOLTS

Description

The Teledyne Semiconductor 823 voltage regulator is constructed on a single monolithic silicon substrate using planar epitaxial techniques. The 823 has a temperature compensated zener referencing the amplifier, an error amplifier and a series pass transistor with current limiting circuitry. An external NPN or PNP pass element may be used when additional output current is required. It can be used as a pin for pin substitute for the 723 voltage regulator in all applications with the additional advantages of lower quiescent current drain, lower drift, improved line regulation, and higher input voltage.

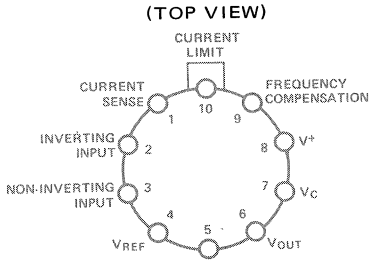
Equivalent Circuit Diagram



L Package pinouts in parentheses.
*V_Z connection in L Package only.

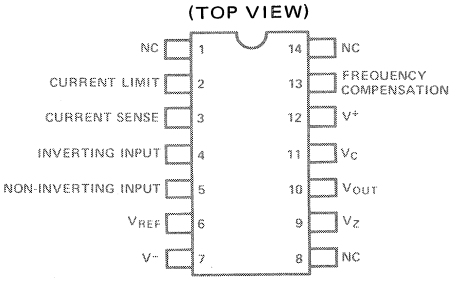
Connection Diagrams

E PACKAGE
10 LEAD METAL CAN
(TOP VIEW)



Order Part Numbers:
823AE, 823BE

L PACKAGE
14 LEAD CERDIP
(TOP VIEW)



Order Part Numbers:
823AL, 823BL

Absolute Maximum Ratings

	823A	823B
Input-Output Voltage Differential	40V	40V
Maximum Output Current	150mA	150mA
Continuous Voltage from V^+ to V^-	50V	40V
Current from V_{REF}	15mA	15mA
Current from V_Z	25mA	25mA
Internal Power Dissipation (Note 1) "E" Package	800mW	800mW
"L" Package	900mW	900mW
Operating Temperature Range	-55°C/+125°C	-55°C/+125°C
Storage Temperature Range	-65°C/+150°C	-65°C/+150°C
Lead Temperature (Soldering, 60 sec.)	300°C	300°C

Electrical Characteristics

Parameter	Conditions	823A			823B			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Line Regulation (Note 2)	V_{IN} = 12V to V_{IN} = 15V		0.01	0.02		0.01	0.05	$\%V_{OUT}$
	V_{IN} = 12V to V_{IN} = 40V		0.02	0.1		0.1	0.2	$\%V_{OUT}$
	$-55°C \leq T_A \leq +125°C$, V_{IN} = 12V to V_{IN} = 15V			0.05				$\%V_{OUT}$
	$0°C \leq T_A \leq 70°C$, V_{IN} = 12V to V_{IN} = 15V						0.1	$\%V_{OUT}$
Load Regulation (Note 2)	I_L = 1 mA to I_L = 50 mA		0.03	0.1		0.03	0.2	$\%V_{OUT}$
	$-55°C \leq T_A \leq +125°C$, I_L = 1 mA to I_L = 50mA			0.2				
	$0°C \leq T_A \leq 70°C$, I_L = 1 mA to I_L = 50 mA						0.4	$\%V_{OUT}$
Ripple Rejection	f = 50 Hz to 10 kHz, C_{REF} = 0	70	74		60	74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF	76	86		66	86		dB
Average Temperature Coefficient of Output Voltage	$-55°C \leq T_A \leq +125°C$		0.002	0.005				%/°C
	$0°C \leq T_A \leq 70°C$					0.003	0.015	%/°C
Short Circuit Current Limit	R_{SC} = 10Ω, V_{OUT} = 0		65			65		mA
Reference Voltage		6.95	7.15	7.35	6.80	7.15	7.50	V
Output Noise Voltage	BW =100 Hz to 10 kHz, C_{REF} = 0		20			20		μV_{rms}
	BW =100 Hz to 10 kHz, C_{REF} = 5 μF		2.5			2.5		μV_{rms}
Long Term Stability			0.1			0.1		%/1000 hrs
Standby Current Drain	I_L = 0, V_{IN} = 40V					0.8	2.0	mA
	I_L = 0, V_{IN} = 50V		0.8	1.5				mA
Input Voltage Range		9.5		50	9.5		40	V
Output Voltage Range		2.0		40	2.0		37	V
Input-Output Voltage Differential	I_L = 0 mA	2.5		40	2.5		38	V
	I_L = 50 mA	3.0		15	3.0		15	V

NOTES:

1. Derate linearly at 6.8mW/°C for metal can package and at 9mW/°C for the ceramic dual-in-line for operation at ambient temperatures above 25°C.
2. At T_A = 25°C, V_{IN} = V^+ = V_C = 12V, V^- = 0, V_{OUT} = 5V, I_L = 1mA, R_{SC} = 0, C_1 = 100pF [C_1 compensation capacitor — Pins 9 (13) to Pins 2 (4).], C_{REF} = 0 and divider impedance as seen by error amplifier ≤ 10K (unless otherwise specified). Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high power dissipation.

829/830

Three-Terminal Positive Voltage Regulators

Features

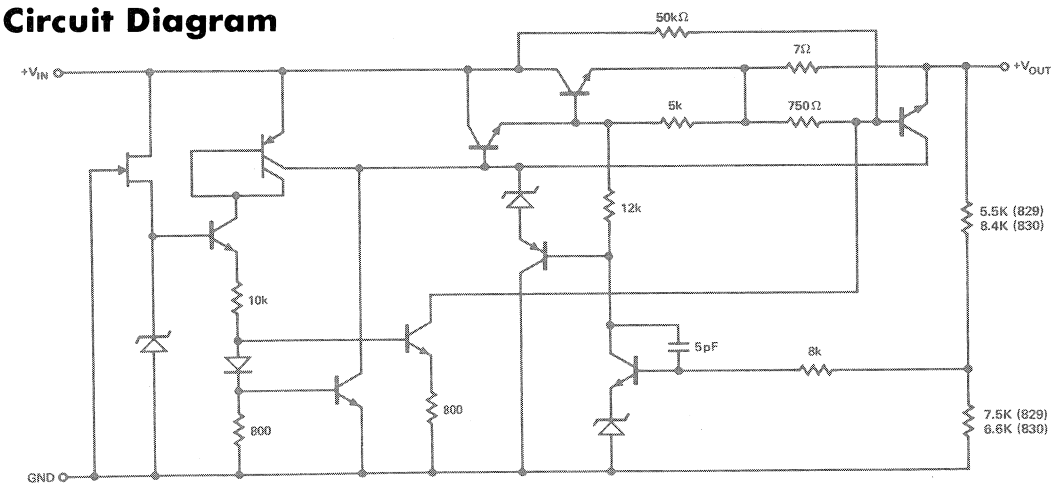
- AVAILABLE FOR 12V (829) OR 15V (830) OPERATION
- LOW COST
- SMALL SIZE PERMITS "ON BOARD" REGULATION
- PERFECT FOR 12V OR 15V HiNIL AND 74C LOGIC SUPPLIES
- 50mA OUTPUT
- EASILY EXPANDABLE TO HIGHER OUTPUT CURRENTS
- INTERNAL CURRENT LIMITING AND THERMAL CONTROL CIRCUITRY

Description

The Teledyne 829 and 830 voltage regulators are low cost three-terminal spot regulators constructed on a single monolithic substrate using epitaxial techniques. The 829 is for 12 volt operation, and the 830 is a 15 volt version. Intended to be the lowest cost solution to commercial/ industrial problems, they are ideal both for op-amp power supplies and as "minimum component" power supplies for 12V or 15V logic such as Teledyne HiNIL or 74C. The number of external components has been minimized by placing all components on the chip. If the regulator is some distance away from the filter capacitors, external bypass capacitors may be needed on the input and output. The current capability of the circuit can be considerably extended through the use of discrete output transistors.

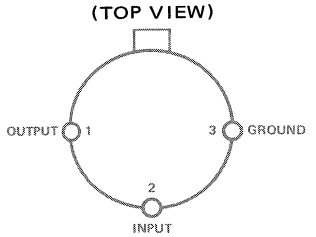
The 829BE and 830BE are intended for operation from −55°C to +125°C. The 829CE and 830CE operate from 0°C to +70°C.

Equivalent Circuit Diagram



Connection Diagram

E PACKAGE
3 LEAD METAL CAN
(TOP VIEW)



Order Part Numbers:
892BE, 830BE (−55°C/+125°C)
830BE, 830CE (−30°C/+70°C)

Absolute Maximum Ratings

	829B, 830B	829C, 830C
Differential Input Output Voltage	35V	30V
Peak Output Current	100mA	100mA
Pulse Voltage from V_{IN} to Gnd (50ms)	45V	35V
Continuous Voltage from V_{IN} to Gnd	40V	30V
Internal Power Dissipation (Note 1)	1000mW	1000mW
Storage Temperature Range	-65°C/+150°C	-65°C/+100°C
Operating Temperature Range	-55°C/+125°C	0°C/+70°C
Lead Soldering Temperature (60 sec)	300°C	300°C
Junction Temperature	150°C	100°C

The above ratings are not meant to imply operation at all of these extremes simultaneously. Exceeding any or all of the absolute maximum ratings may cause permanent damage to the device.

NOTE: 1. For operation at elevated temperatures, the devices must be derated by the thermal resistance method (TO-5. . .125°C/W, junction to ambient, or 25°C/W junction to case.

Electrical Characteristics

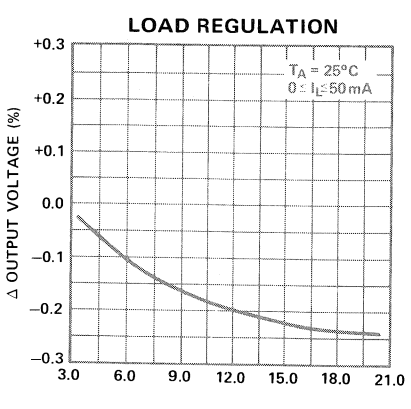
PARAMETER	CONDITIONS	829B			830B			829C			830C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_{IN} = 20V ±.25V T_J = 25°C	11.4	12	12.6	14.4	15.0	15.6	11.25	12	12.75	14.25	15.0	15.75	V
Line Regulation	20V ≤ V_{IN} ≤ 22V T_J = 25°C		10	18		10	25		12	18		15	25	mV
	20V ≤ V_{IN} ≤ 30V T_J = 25°C		15	60		10	80		30	72		20	95	mV
	20V ≤ V_{IN} ≤ 22V T_{MIN} ≤ T_A ≤ T_{MAX}			72			95			72			95	mV
Load Regulation	V_{IN} = 24V ± .25V 1mA ≤ I_L ≤ 50mA T_J = 25°C		12	24		15	31		15	30		20	40	mV
	T_{MIN} ≤ T_A ≤ T_{MAX}			72			95			72			95	mV
Ripple Rejection	V_{RIP} = 1V_{pp} 50Hz ≤ f ≤ 10KHz V_{IN} = 24V ± .25V T_{MIN} ≤ T_A ≤ T_{MAX}			0.01			0.01			0.01			0.01	V
Loaded Output Voltage	20V ≤ V_{IN} ≤ 30V 1mA ≤ I_L ≤ 50mA V_{RIP} = 1.0V_{pp} 50Hz ≤ f ≤ 10KHz T_{MIN} ≤ T_A ≤ T_{MAX}	11		13	14		16	11		13	14		16	V
Input Voltage Range	T_{MIN} ≤ T_A ≤ T_{MAX}	15		40	18		40	15		30	18		30	V
Quiescent Current	20V ≤ V_{IN} ≤ 30V T_{MIN} ≤ T_A ≤ T_{MAX}		4.0	6.0		4.0	6.0		4.0	6.0		4.0	6.0	mA

NOTES:

T_{MIN} = -55°C for B versions T_{MAX} = +125°C for B versions

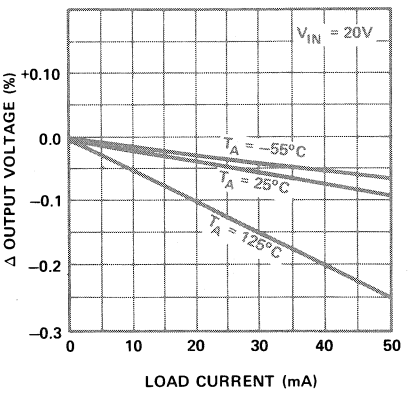
T_{MIN} = 0°C for C versions T_{MAX} = +70°C for C versions

Typical Characteristics

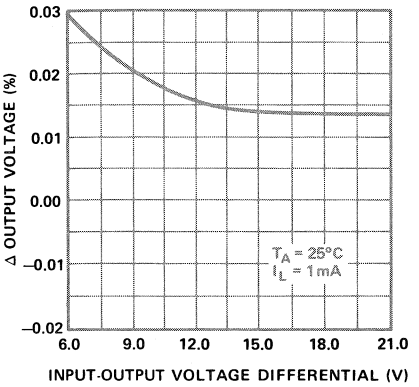


Typical Characteristics (Cont'd.)

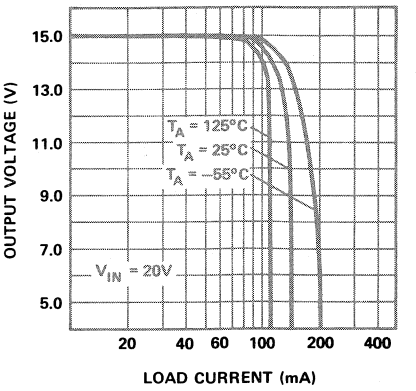
LOAD REGULATION



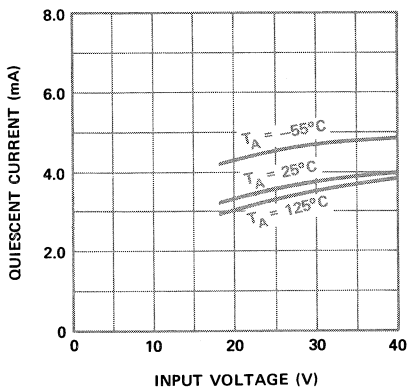
LINE REGULATION



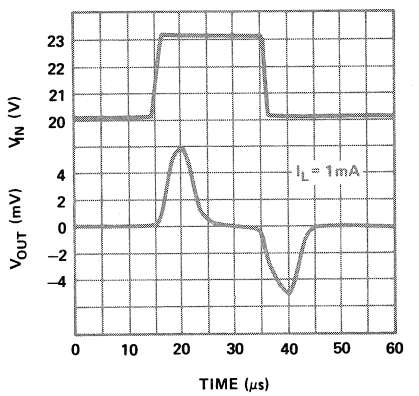
CURRENT LIMITING CHARACTERISTICS



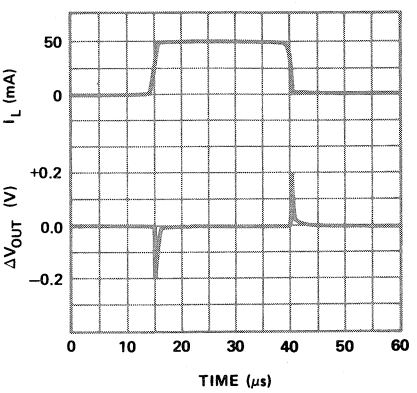
QUIESCENT CURRENT



LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



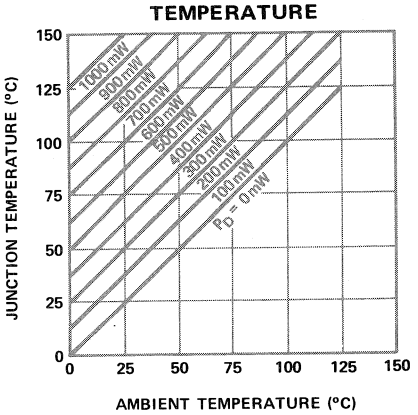
Typical Applications

The Teledyne 829 and 830 three leaded regulators are exceptionally easy to use. By incorporating all of the normally needed external components onto the IC chip, a spot regulator can be built that requires only the bare minimum number of external components. Four designs are presented in 12V and 15V versions: a 50mA regulator, a 1A regulator, a spot regulator featuring load currents in excess of 1A, and a current regulator.

STEP 1. Determine the maximum allowable power dissipation, P_D, from Chart 1. Use the highest ambient temperature in which the device is expected to operate, and the maximum junction temperature permitted (see absolute maximum ratings), and pick off the maximum allowable power dissipation.

EXAMPLE: The regulator will be called on to operate in ambient temperatures of T_A = 75°C max. The junction temperature has been restricted to T_J = 125°C max. The maximum allowable power dissipation, P_D, is 400mW.

CHART 1
METAL CAN JUNCTION TEMPERATURE

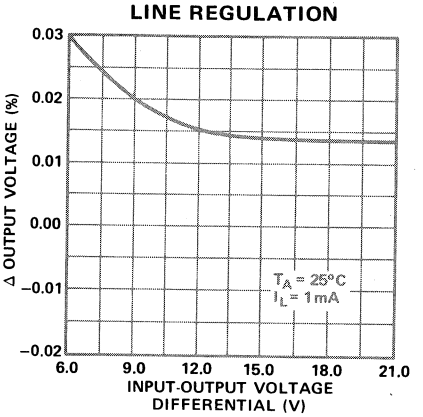


Typical Applications (Cont'd.)

STEP 2. The line regulation is determined primarily by the input-output voltage differential. Pick the typical line regulation your regulator should exhibit and determine from Chart 2 the input/output voltage differential necessary to achieve this performance.

EXAMPLE: The typical line regulation desired for this design is 0.02%. From Chart 2 this corresponds to an input-output voltage differential of 9V.

CHART 2
LINE REGULATION



STEP 3. Calculate the worst case power dissipation attributed to quiescent current. This is determined by multiplying the quiescent current, 6.0 mA, by the input voltage to the regulator.

12V EXAMPLE: In the example of Step 2, the input/output differential was to be 9.0V. That means V_{IN}, the input voltage, must be 12V +9.0V = 21V. P_D (QUIESCENT) [worst case] = 21V X 6.0mA = 126mW.

15V EXAMPLE: In Step 2, the input/output differential was determined to be 9.0V. That means V_{IN}, the input voltage, must be 15V +9V = 24V. P_D (QUIESCENT) [worst case] = 24V X 6.0mA = 144mW.

STEP 4. Calculate the power dissipated by the load. This is done by subtracting the dissipation due to quiescent current (Step 3) from the maximum allowable total dissipation (Step 1).

12V EXAMPLE: If the total power dissipation was determined in Step 1 to be 400mW and the quiescent power dissipation to be 126mW (Step 3), the max. power left for regulation must be 400mW −126mW = 274mW.

15V EXAMPLE: The total power dissipation was determined in Step 1 to be 400mW and the quiescent power dissipation to be 144mW (Step 3). The max. power left for regulation must be 400mW −144mW = 256mW.

STEP 5. Calculate the maximum load current available by dividing the regulation power (Step 4) by the input/output voltage differential (Step 2).

12V EXAMPLE:

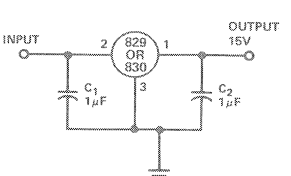
$$\frac{\text{274mW (Regulation Power)}}{\text{9.0V In/Out Diff.}} = 30.44\text{mA } I_L \text{ (Load Current)}$$

15V EXAMPLE:

$$\frac{\text{256mW (Regulation Power)}}{\text{9.0V In/Out Diff.}} = 28.4\text{mA } I_L \text{ (Load Current)}$$

DESIGN A. — LOW CURRENT SPOT REGULATOR

For some applications, the maximum load current determined in Step 5 may be sufficient. In that event, two stabilization capacitors are all that is required to use the 829 or 830 as a spot regulator. If the regulator is physically close to the filter capacitor of the power supply, the input capacitor, C_1, may be omitted.



Typical Applications (Cont'd.)

DESIGN B. – 1A SPOT REGULATOR

For most designs the 25-50mA of allowable load current from the unaided 829 or 830 will not be sufficient. Operation at heavier load currents will require the use of an external pass transistor. The transistor that is chosen must satisfy the following three conditions:

Condition 1. The transistor must be able to dissipate the full load current at the input/output voltage differential.

Condition 2. The transistor must be able to pass collector current equal to the maximum load current.

Condition 3. The h_{fe} of the transistor must be large enough so that using the max. load current determined in Step 5 as a base drive, the transistor will pass the full load current.

The resistor R_1 must be chosen so that the voltage drop across it when passing 15mA must be equal to 0.7V. Note: 15mA must not be larger than the max. load current through the 829 or 830 as determined in Step 5. If it is, design C must be used.

EXAMPLE:

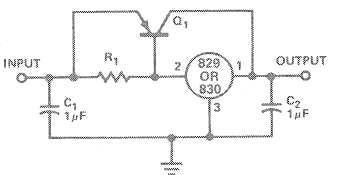
12V or 15V 1 Amp

$$R_1 = \frac{0.7V}{15mA} = 47\Omega$$

Q_1: $I_C \geq 1$ Amp

$$h_{fe} \geq \frac{1\text{ Amp}}{28mA} = 36$$

$P_D \geq 1$ Amp x 9V = 9W



DESIGN C. – REGULATORS – 1 AMP and UP

The limitations of maximum I_L determined in Step 5 and the availability of economical high β power transistors impose a ceiling of about 1 Amp maximum load current for the design B regulator. This can be extended tremendously by using two transistors. The first, Q_1, is selected exactly as in design B where the maximum load current is 1A. Q_2 is selected by the same criteria except that the maximum load current is now the total design value, i.e., 5A. The h_{fe} must then be capable of providing an I_C = 5A with a base drive of 1A. R_2 is chosen so that when .3 X I_{load} (Q_1) is flowing through it, the voltage drop is 0.7V. In some cases, a more economical solution is to use a smaller transistor for Q_1 and a higher β device for Q_2. R_1 is selected as before.

EXAMPLE:

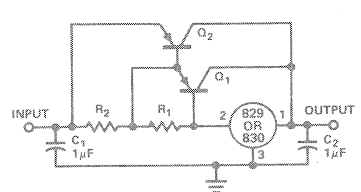
12V or 15V 5 Amp

Q_1: $I_C \geq 1$ Amp
$h_{fe} \geq 36$
$P_D \geq 9W$

Q_2: $I_C \geq 5$ Amp
$h_{fe} \geq 5$
$P_D \geq 45W$

$R_1 = 47\Omega$

$$R_2 = \frac{0.7V}{.3 \times 1A} = 2.3\Omega$$



Typical Applications (Cont'd.)

DESIGN D. – CURRENT REGULATOR

The 829 or 830 can be made to function as a current regulator by the circuit shown below. It will operate between the minimum/maximum values of input/output voltage differential and between maximum load current and the quiescent operating current.

EXAMPLE:

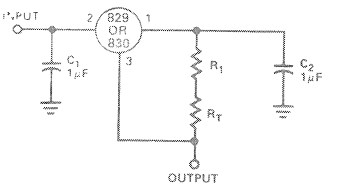
At 12V:

$$I_{OUT} = I_{QUIESCENT} + \frac{12V}{R_1 + R_T}$$

At 15V:

$$I_{OUT} = I_{QUIESCENT} + \frac{15V}{R_1 + R_T}$$

R_T is included to trim out the effects of variations in the quiescent current from unit to unit.



78M00 Series*

Three-Terminal Positive Voltage Regulators

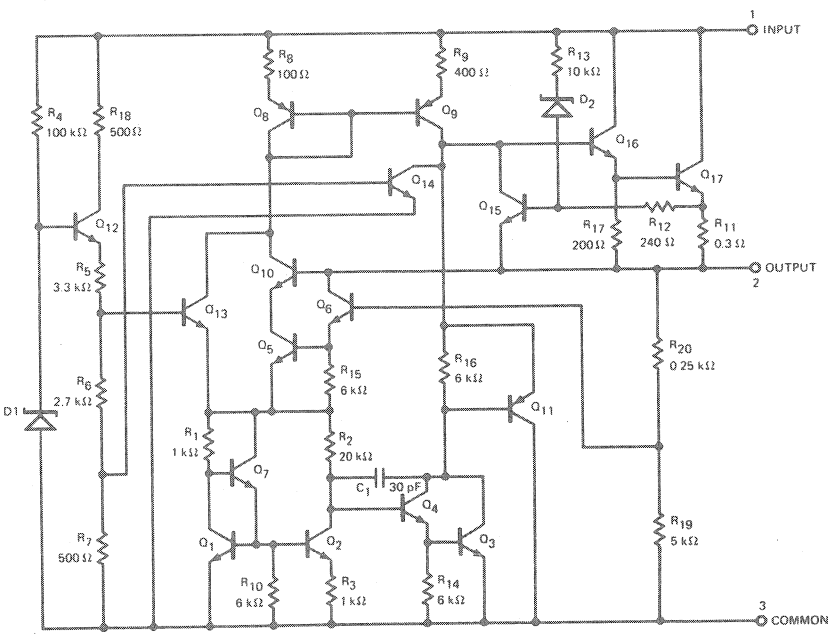
Features

- OUTPUT CURRENT UP TO 0.5 AMP
- NO EXTERNAL COMPONENTS
- INTERNAL THERMAL OVERLOAD PROTECTION
- INTERNAL SHORT CIRCUIT CURRENT LIMITING
- OUTPUT TRANSISTOR SAFE-AREA COMPENSATION

Description

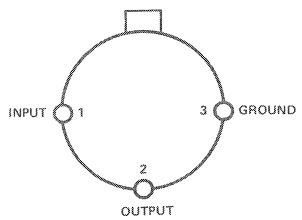
The Teledyne 78M00 series of three-terminal medium current positive voltage regulators employ internal current limiting, thermal shutdown and safe-area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver up to 500mA output current. Intended as fixed-voltage regulators, they can be used in a wide range of applications including local, on-card regulation for elimination of noise and distribution problems associated with single point regulation. In addition to fixed voltage regulator applications, these devices can be used with external components to obtain adjustable output voltages and currents and as the power pass element in precision regulators.

Schematic Diagrams



Connection Diagram

E PACKAGE
3 LEAD METAL CAN
(TOP VIEW)



ORDER INFORMATION

OUTPUT VOLTAGE	PART NO.	OUTPUT VOLTAGE	PART NO.
5V	78M05BE	5V	78M05CE
6V	78M06BE	6V	78M06CE
8V	78M08BE	8V	78M08CE
12V	78M12BE	12V	78M12CE
15V	78M15BE	15V	78M15CE
20V	78M20BE	20V	78M20CE
24V	78M24BE	24V	78M24CE

*available soon

Absolute Maximum Ratings

Input Voltage	
(5V, 6V, 8V)	30V
(12V, 15V)	35V
(20V, 24V)	40V
Internal Power Dissipation (Note 1)	Internally Limited
Storage Temperature Range	−65°C to +200°C
Operating Temperature Range (Note 2)	
Military (78M00)	−55°C to +150°C
Commercial (78M00C)	0°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

NOTES:

1. Thermal resistance of the packages (without a heat sink): Junction to Case — 20°C/W; Junction to Ambient — 150°C/W
2. Operating Ambient Temperature Range: 78M00B — −55°C to +125°C; 78M00C — 0°C to +85°C.

Electrical Characteristics

78M05

(V_{IN} = 10V, I_{OUT} = 200mA, −55°C ≤ T_J ≤ 150°C for 78M05B and 0°C ≤ T_J ≤ 150°C for 78M05C, unless otherwise specified).

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C		5.0		V
Line Regulation	T_J = 25°C 7V ≤ V_{IN} ≤ 25V		3.0		mV
Load Regulation	T_J = 25°C 5mA ≤ I_{OUT} ≤ 0.5A		25		mV
Output Voltage	8.0V ≤ V_{IN} ≤ 25V 5mA ≤ I_{OUT} ≤ 200mA		5.0		V
Quiescent Current	T_J = 25°C		4.5		mA
Quiescent Current Change with line	8V ≤ V_{IN} ≤ 25V		0.2		mA
Quiescent Current Change with load	5mA ≤ I_{OUT} ≤ 200mA		0.1		mA
Output Noise Voltage	T_A = 25°C, 10Hz ≤ f ≤ 100kHz		40		μV
Ripple Rejection	f = 120Hz, 8V ≤ V_{IN} ≤ 18V I_{OUT} = 300mA, T_J = 25°C		78		dB
Dropout Voltage	T_J = 25°C		2.0		V
Peak Output Current	T_J = 25°C		700		mA

78M06

(V_{IN} = 11V, I_{OUT} = 200mA, −55°C ≤ T_J ≤ 150°C for 78M06B and 0°C ≤ T_J ≤ 150°C for 78M06C, unless otherwise specified).

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C		6.0		V
Line Regulation	T_J = 25°C 8V ≤ V_{IN} ≤ 25V		5.0		mV
Load Regulation	T_J = 25°C 5mA ≤ I_{OUT} ≤ 0.5A		30		mV
Output Voltage	9V ≤ V_{IN} ≤ 25V 5mA ≤ I_{OUT} ≤ 200mA		6.0		V
Quiescent Current	T_J = 25°C		4.5		mA
Quiescent Current Change with line	9V ≤ V_{IN} ≤ 25V		0.2		mA
Quiescent Current Change with load	5mA ≤ I_{OUT} ≤ 200mA		0.1		mA
Output Noise Voltage	T_A = 25°C, 10Hz ≤ f ≤ 100kHz		45		μV
Ripple Rejection	f = 120Hz, 9V ≤ V_{IN} ≤ 19V I_{OUT} = 300mA, T_J = 25°C		75		dB
Dropout Voltage	T_J = 25°C		2.0		V
Peak Output Current	T_J = 25°C		700		mA

Electrical Characteristics (Cont'd.)

78M08

(V_{IN} = 14V, I_{OUT} = 200mA, −55°C ≤ T_J ≤ 150°C for 78M08B and 0°C ≤ T_J ≤ 150°C for 78M08C, unless otherwise specified).

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C		8.0		V
Line Regulation	T_J = 25°C 10.5V ≤ V_{IN} ≤ 25V		6.0		mV
Load Regulation	T_J = 25°C 5mA ≤ I_{OUT} ≤ 0.5A		40		mV
Output Voltage	11.5V ≤ V_{IN} ≤ 23V 5mA ≤ I_{OUT} ≤ 200mA		8.0		V
Quiescent Current	T_J = 25°C		4.6		mA
Quiescent Current Change with line	11.5V ≤ V_{IN} ≤ 25V		0.2		mA
Quiescent Current Change with load	5mA ≤ I_{OUT} ≤ 200mA		0.1		mA
Output Noise Voltage	T_A = 25°C, 10Hz ≤ f ≤ 100kHz		52		μA
Ripple Rejection	f = 120Hz, 11.5V ≤ V_{IN} ≤ 21.5V I_{OUT} = 300mA, T_J = 25°C		72		dB
Dropout Voltage	T_J = 25°C		2.0		V
Peak Output Current	T_J = 25°C		750		mA

78M12

(V_{IN} = 19V, I_{OUT} = 200mA, −55°C ≤ T_J ≤ 150°C for 78M12B and 0°C ≤ T_J ≤ 150°C for 78M12C, unless otherwise specified).

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C		12		V
Line Regulation	T_J = 25°C 14.5V ≤ V_{IN} ≤ 30V		10		mV
Load Regulation	T_J = 25°C 5mA ≤ I_{OUT} ≤ 0.5A		50		mV
Output Voltage	15.5V ≤ V_{IN} ≤ 27V 5mA ≤ 200mA		12		V
Quiescent Current	T_J = 25°C		4.8		mA
Quiescent Current Change with line	15V ≤ V_{IN} ≤ 30V		0.2		mA
Quiescent Current Change with load	5mA ≤ I_{OUT} ≤ 200mA		0.1		mA
Output Noise Voltage	T_A = 25°C, 10Hz ≤ f ≤ 100kHz		75		μA
Ripple Rejection	f = 120Hz, 15V ≤ V_{IN} ≤ 25V I_{OUT} = 300mA, T_J = 25°C		71		dB
Dropout Voltage	T_J = 25°C		2.0		V
Peak Output Current	T_J = 25°C		700		mA

78M15

(V_{IN} = 23V, I_{OUT} = 200mA, −55°C ≤ T_J ≤ 150°C for 78M15B and 0°C ≤ T_J ≤ 150°C for 78M15C, unless otherwise specified).

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C		15		V
Line Regulation	T_J = 25°C 17.5V ≤ V_{IN} ≤ 30V		11		mV
Load Regulation	T_J = 25°C 5mA ≤ I_{OUT} ≤ 0.5A		60		mV
Output Voltage	18.5V ≤ V_{IN} ≤ 30V 5mA ≤ I_{OUT} ≤ 200mA		15		V
Quiescent Current	T_J = 25°C		4.8		mA
Quiescent Current Change with line	18.5V ≤ V_{IN} ≤ 30V		0.2		mA
Quiescent Current Change with load	5mA ≤ I_{OUT} ≤ 200mA		0.1		mA
Output Noise Voltage	T_A = 25°C, 10Hz ≤ f ≤ 100kHz		90		μV
Ripple Rejection	f = 120Hz, 18.5V ≤ V_{IN} ≤ 28.5V I_{OUT} = 300mA, T_J = 25°C		70		dB
Dropout Voltage	T_J = 25°C		2.0		V
Peak Output Current	T_J = 25°C		700		mA

Electrical Characteristics (Cont'd.)

78M20

(V_{IN} = 29V, I_{OUT} = 200mA, −55°C ≤ T_J ≤ 150°C for 78M20B and 0°C ≤ T_J ≤ 150°C for 78M20C, unless otherwise specified).

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C		20		V
Line Regulation	T_J = 25°C 23V ≤ V_{IN} ≤ 36V		15		mV
Load Regulation	T_J = 25°C 5mA ≤ I_{OUT} ≤ 0.5A		80		mV
Output Voltage	24V ≤ V_{IN} ≤ 35V 5mA ≤ I_{OUT} ≤ 200mA		20		V
Quiescent Current	T_J = 25°C		4.9		mA
Quiescent Current Change with line	24V ≤ V_{IN} ≤ 35V		0.2		mA
Quiescent Current Change with load	5mA ≤ I_{OUT} ≤ 200mA		0.1		mA
Output Noise Voltage	T_A = 25°C, 10Hz ≤ f ≤ 100kHz		110		μA
Ripple Rejection	f = 120Hz, 24V ≤ V_{IN} ≤ 34V I_{OUT} = 300mA, T_J = 25°C		69		dB
Dropout Voltage	T_J = 25°C		2.0		V
Peak Output Current	T_J = 25°C		700		mA

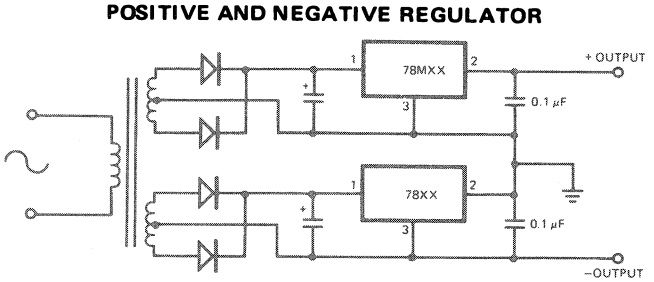
78M24

(V_{IN} = 33V, I_{OUT} = 200mA, −55°C ≤ T_J ≤ 150°C for 78M24B and 0°C ≤ T_J ≤ 150°C for 78M24C, unless otherwise specified).

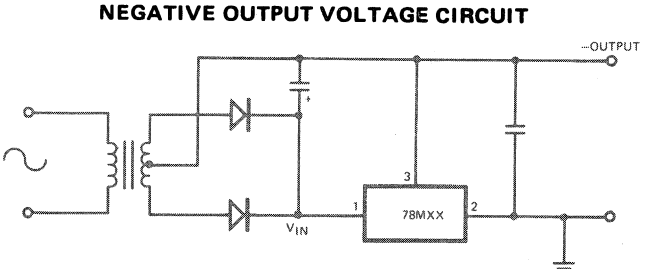
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C		24		V
Line Regulation	T_J = 25°C 27V ≤ V_{IN} ≤ 38V		18		mV
Load Regulation	T_J = 25°C 5mA ≤ I_{OUT} ≤ 0.5A		100		mV
Output Voltage	28V ≤ V_{IN} ≤ 38V 5mA ≤ I_{OUT} ≤ 200mA		24		V
Quiescent Current	T_J = 25°C		5.0		mA
Quiescent Current Change with line	28V ≤ V_{IN} ≤ 38V		0.2		mA
Quiescent Current Change with load	5mA ≤ I_{OUT} ≤ 200mA		0.1		mA
Output Noise Voltage	T_A = 25°C. Hz ≤ f ≤ 100kHz		170		μV
Ripple Rejection	f = 120Hz, 28V ≤ V_{IN} ≤ 38V I_{OUT} = 300mA, T_J = 25°C		66		dB
Dropout Voltage	T_J = 25°C		2.0		V
Peak Output Current	T_J = 25°C		700		mA

Typical Applications

POSITIVE AND NEGATIVE REGULATOR

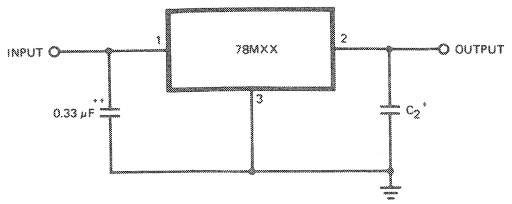


NEGATIVE OUTPUT VOLTAGE CIRCUIT



Typical Applications (Cont'd.)

FIXED OUTPUT REGULATOR



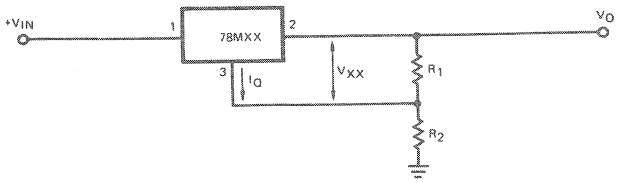
NOTES:

* To specify an output voltage, substitute voltage value for "XX."

\+ Although no output capacitor is needed for stability, it does improve transient response.

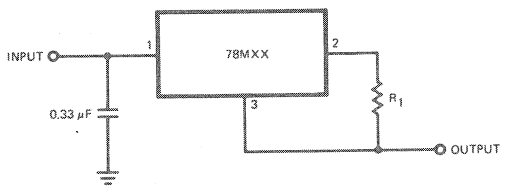
++ Required if regulator is located an appreciable distance from power supply filter.

CIRCUIT FOR INCREASING OUTPUT VOLTAGE



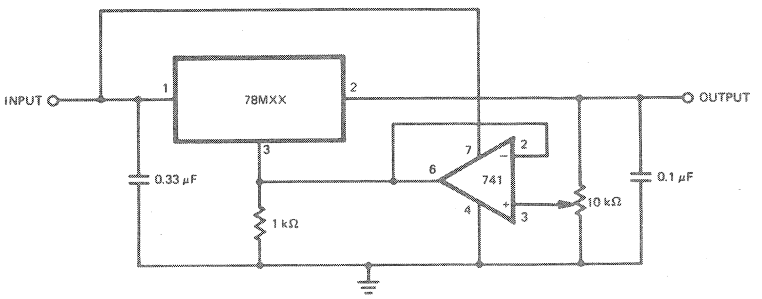
$$V_O = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + I_Q R_2$$

CURRENT REGULATOR

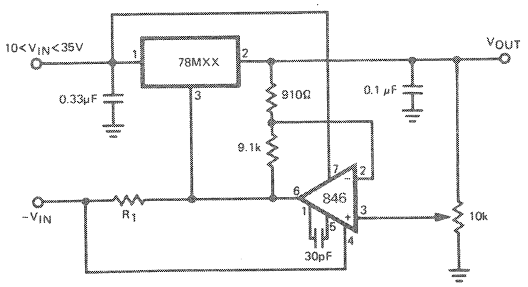


$$\text{Output Current} = \frac{V_{OUT}}{R_1}$$

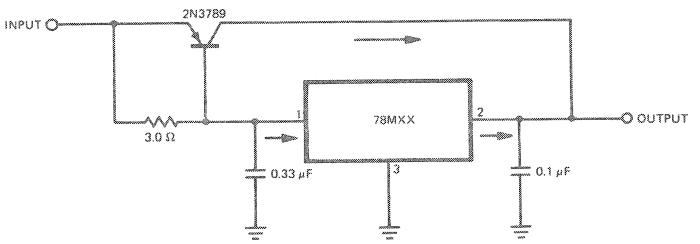
ADJUSTABLE OUTPUT REGULATOR, 7 to 30 VOLTS



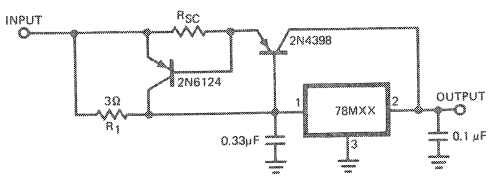
VARIABLE OUTPUT VOLTAGE, 0.5 to 7 VOLTS



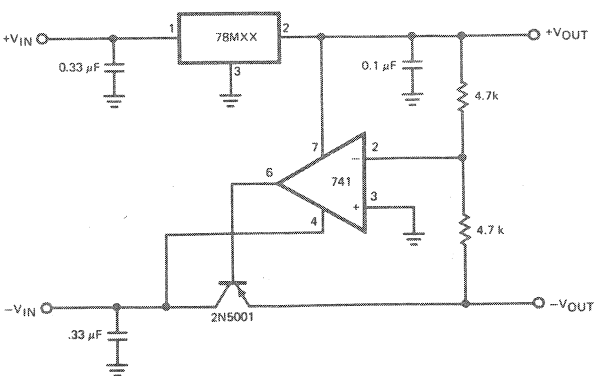
HIGH CURRENT VOLTAGE REGULATOR



HIGH OUTPUT CURRENT, SHORT CIRCUIT PROTECTED



± TRACKING VOLTAGE REGULATOR



Section IV

Comparators and Peripheral Drivers

111 Series

111 • 211 • 311
Voltage Comparators

Features

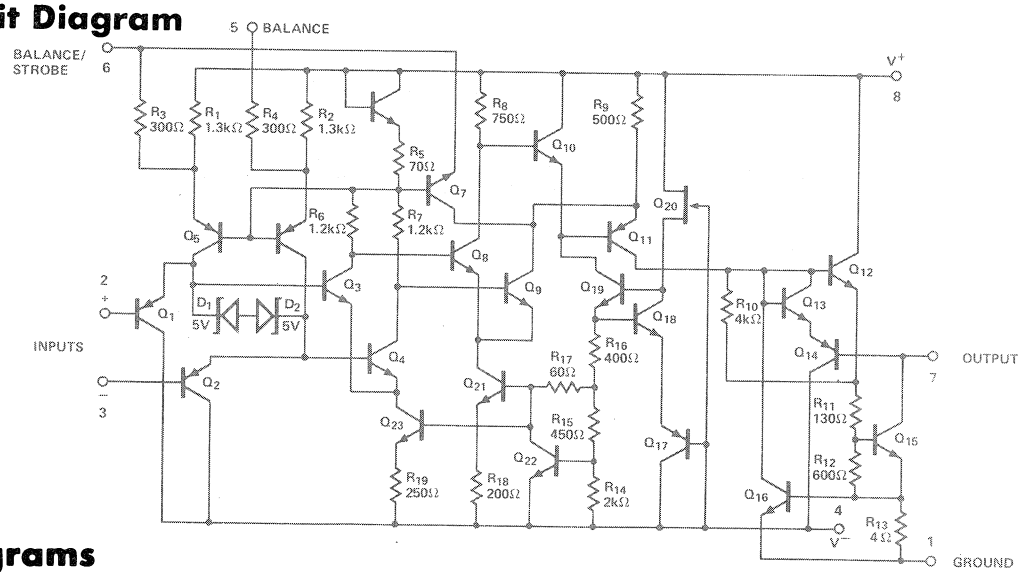
- LOW INPUT BIAS CURRENT – 60nA
- LOW INPUT OFFSET CURRENT – 4nA
- DIFFERENTIAL INPUT VOLTAGE – ±30V
- OPERATION FROM SINGLE 5.0V TO ±15V POWER SUPPLIES
- OFFSET VOLTAGE NULL CAPABILITY
- STROBE CAPABILITY
- VERSATILE OUTPUT STAGE

Description

The Teledyne 111 Series high performance comparator is constructed on a single monolithic silicon substrate using planar epitaxial techniques. The device can operate from a single +5V supply used for integrated circuit logic as well as conventional ±15V supplies used in systems with operational amplifiers. The 111 series is intended for a wide range of applications including driving lamps or relays and switching output voltages up to 50V at currents as high as 50mA. The extremely versatile output stage is compatible with DTL, TTL, CMOS, and MOS logic families.

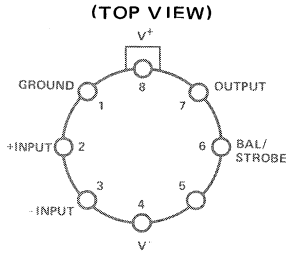
The 111 operates over the full military temperature range of −55°C to +125°C. The 211 is the same as the 111 except its performance is guaranteed from −25°C to +85°C. The 311 is the commercial version which operates from 0°C to +70°C.

Equivalent Circuit Diagram



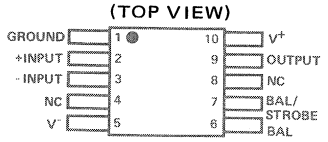
Connection Diagrams

E PACKAGE
8 LEAD METAL CAN
(TOP VIEW)



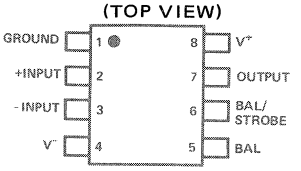
Order Part Numbers:
LM111H, LM211H,
LM311H

H PACKAGE
10 LEAD FLATPACK
(TOP VIEW)



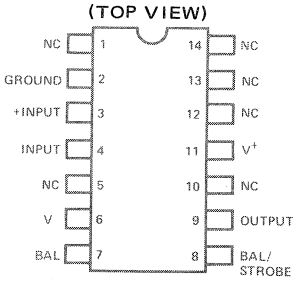
Order Part Number:
LM111F

P PACKAGE
8 LEAD MINIDIP
(TOP VIEW)



Order Part Number:
LM311N

L PACKAGE
14 LEAD CERDIP
(TOP VIEW)



Order Part Numbers:
LM111D, LM211D,
LM311D

Absolute Maximum Ratings

Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Output to V^-	
111	50V
311	40V
Output Short Circuit Duration	10 seconds
Voltage Between V^+ and V^- Terminals	36V
Ground to V^-	30V
Internal Power Dissipation (Note 2)	500mW
Storage Temperature Range	−65°C/+150°C
Operating Temperature Range	
Military (111)	−55°C/+125°C
Commercial (311)	0°C/+70°C

Electrical Characteristics

Unless otherwise specified, $V_S = \pm 15V$, $T_A = -55°C$ to $+125°C$ for 111, $T_A = 0°C$ to $70°C$ for 311. See Note 3.

PARAMETER	CONDITIONS	111		311		UNITS
		TYP.	MAX.	TYP.	MAX.	
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k\Omega$	0.7	3.0	2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$	4.0	10	6.0	50	nA
Input Bias Current	$T_A = 25°C$	60	100	100	250	nA
Voltage Gain	$T_A = 25°C$	200		200		V/mV
Response Time (Note 5)	$T_A = 25°C$	200		200		ns
Saturation Voltage (111)	$V_{IN} \leq -5mV$, $I_{OUT} = 50mA$, $T_A = 25°C$	0.75	1.5			V
Saturation Voltage (311)	$V_{IN} \leq -10mV$, $I_{OUT} = 50mA$, $T_A = 25°C$			0.75	1.5	V
Strobe On Current	$T_A = 25°C$	3.0		3.0		mA
Output Leakage Current	$V_{IN} \geq 5mV$, $V_{OUT} = 35V$, $T_A = 25°C$	0.2	10			nA
Output Leakage Current	$V_{IN} \geq 10mV$, $V_{OUT} = 35V$, $T_A = 25°C$			0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k\Omega$		4.0		10	mV
Input Offset Current (Note 4)			20		70	nA
Input Bias Current			150		300	nA
Input Voltage Range		±14		±14		V
Saturation Voltage (111)	$V+ \geq 4.5V$, $V- = 0$, $V_{IN} \leq -6mV$, $I_{SINK} \leq 8mA$	0.23	0.4			V
Saturation Voltage (311)	$V+ \geq 4.5V$, $V- = 0$, $V_{IN} \leq -10mV$, $I_{SINK} \leq 8mA$			0.23	0.4	V
Output Leakage Current	$V_{IN} \geq 5mV$, $V_{OUT} = 35V$	0.1	0.5			μA
Positive Supply Current	$T_A = 25°C$	5.1	6.0	5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$	4.1	5.0	4.1	5.0	mA

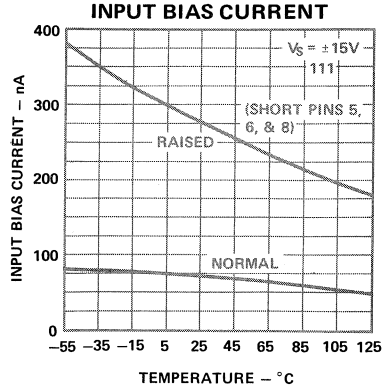
NOTES:

1. This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.
2. The maximum junction temperature of the 111 is 150°C, while that of the 211 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
3. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified (see definitions) is for a 100mV input step with 5mV overdrive.

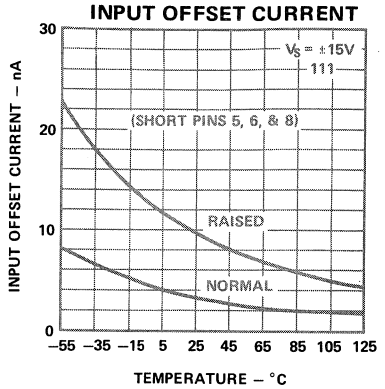
Typical Characteristics

111

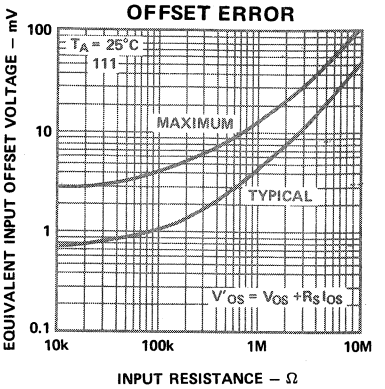
INPUT BIAS CURRENT



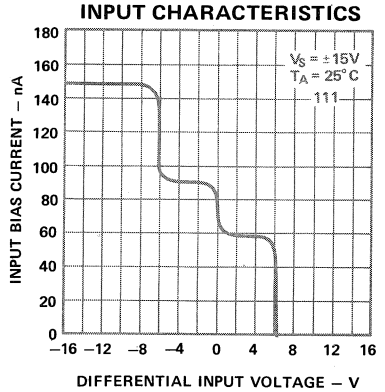
INPUT OFFSET CURRENT



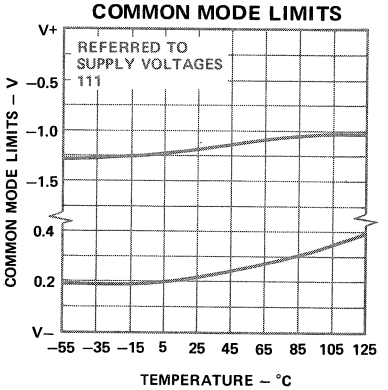
OFFSET ERROR



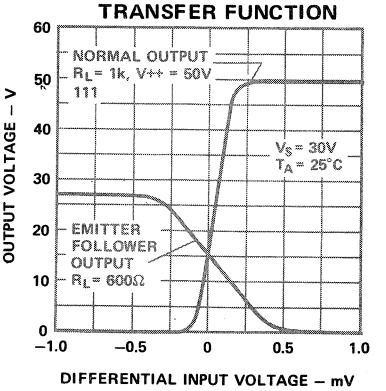
INPUT CHARACTERISTICS



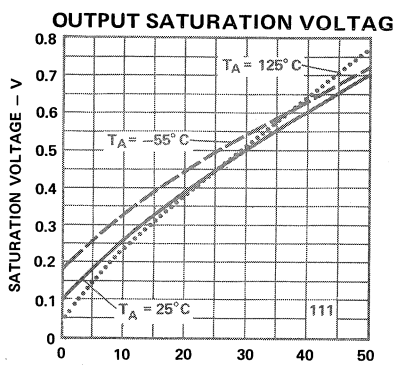
COMMON MODE LIMITS



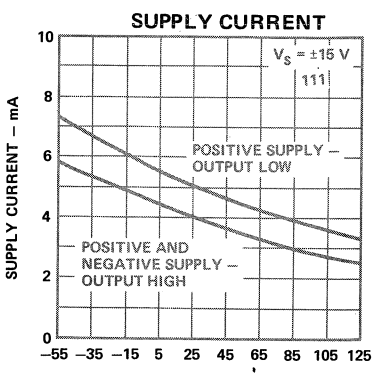
TRANSFER FUNCTION



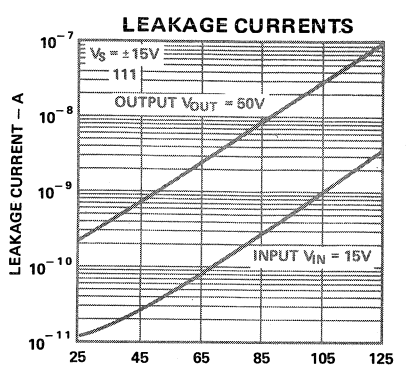
OUTPUT SATURATION VOLTAGE



SUPPLY CURRENT



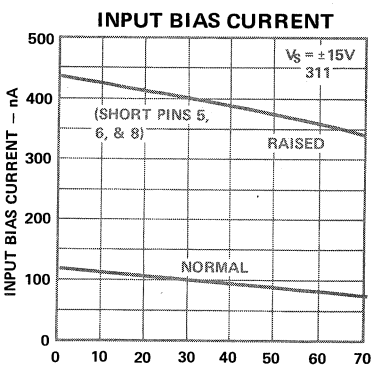
LEAKAGE CURRENTS



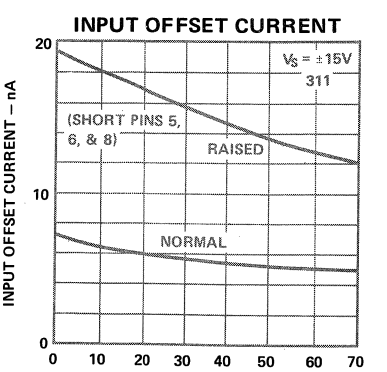
Typical Characteristics

311

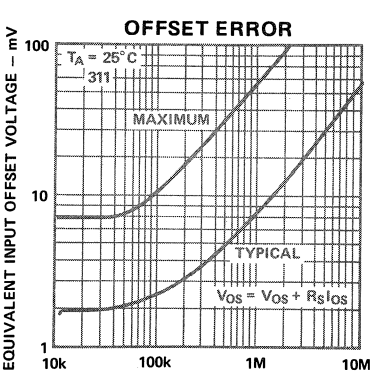
INPUT BIAS CURRENT



INPUT OFFSET CURRENT



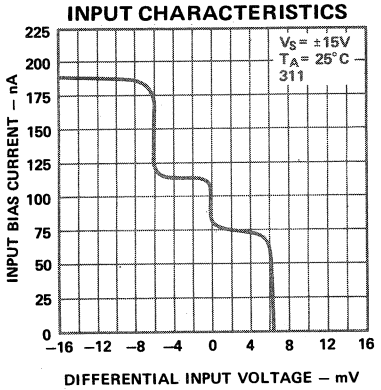
OFFSET ERROR



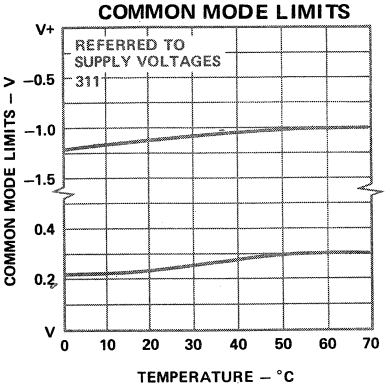
Typical Characteristics (Cont'd.)

311

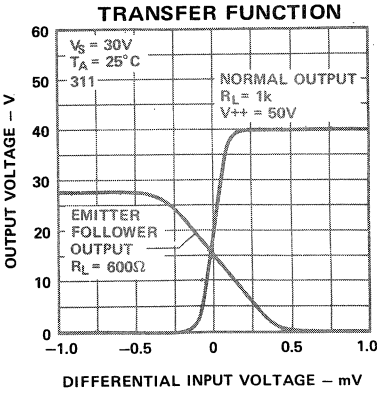
INPUT CHARACTERISTICS



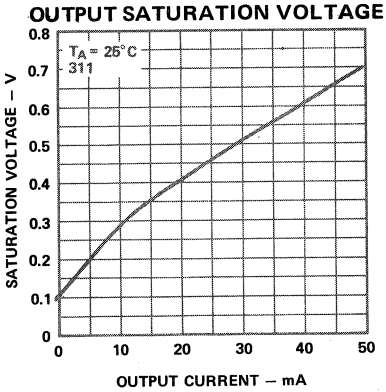
COMMON MODE LIMITS



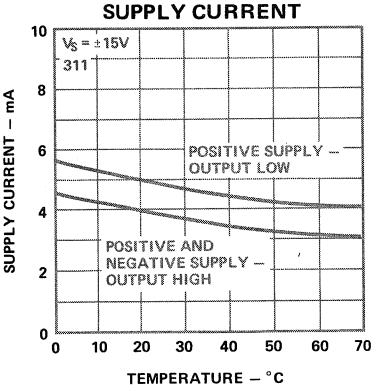
TRANSFER FUNCTION



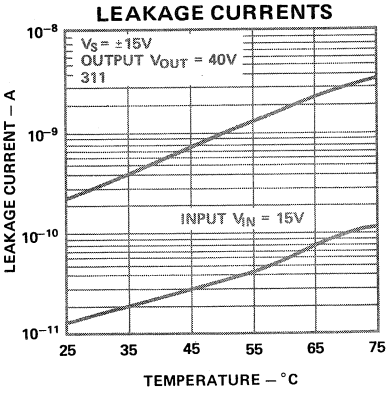
OUTPUT SATURATION VOLTAGE



SUPPLY CURRENT



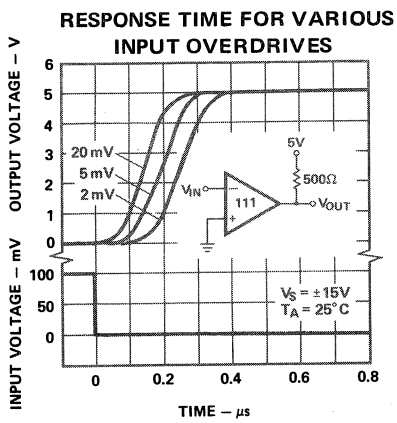
LEAKAGE CURRENTS



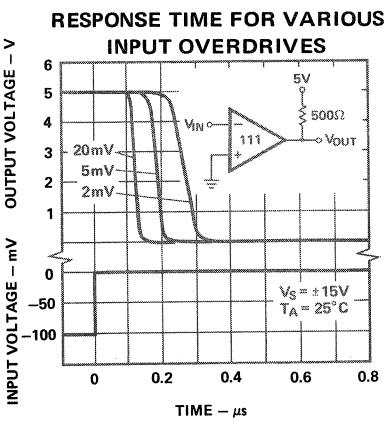
Typical Characteristics

111/311

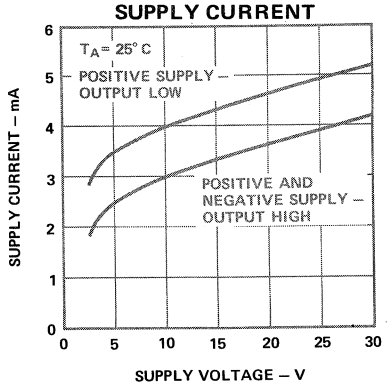
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



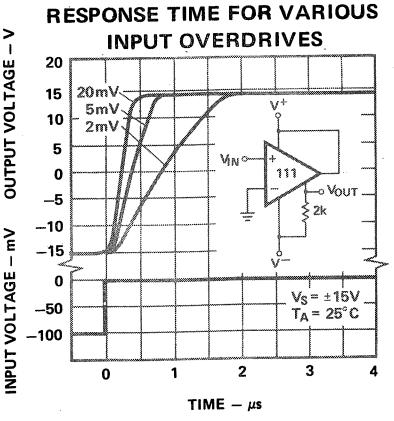
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



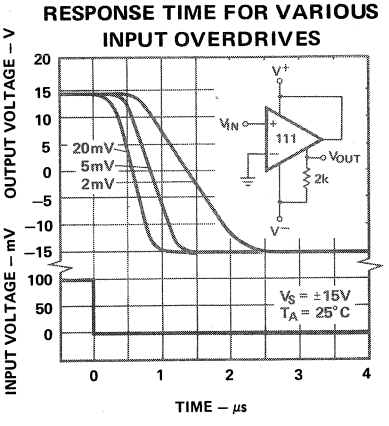
SUPPLY CURRENT



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

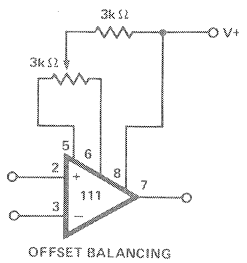


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

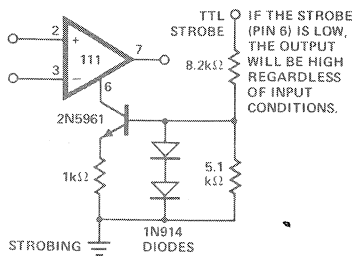


Typical Applications

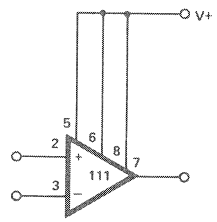
OFFSET NULL CIRCUIT



STROBE CIRCUIT

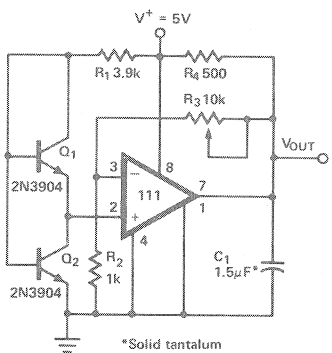


INCREASING INPUT STAGE CURRENT*



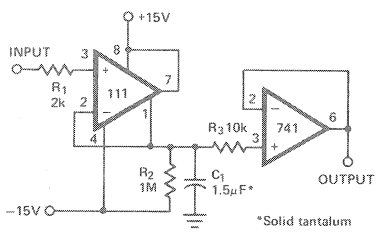
*Increases typical common mode slew rate from 7.0V/μs to 18V/μs.

ADJUSTABLE LOW VOLTAGE REFERENCE SUPPLY



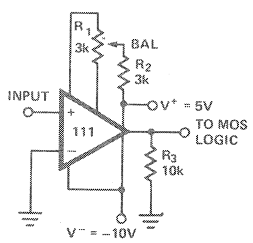
*Solid tantalum

POSITIVE PEAK DETECTOR

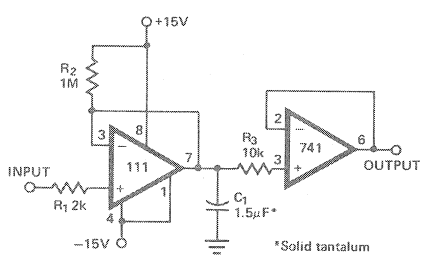


*Solid tantalum

ZERO CROSSING DETECTOR DRIVING MOS LOGIC

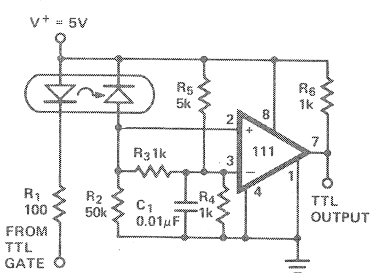


NEGATIVE PEAK DETECTOR

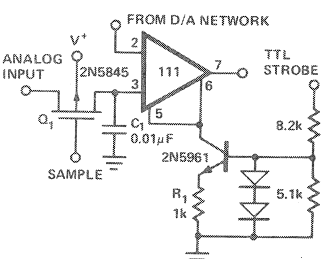


*Solid tantalum

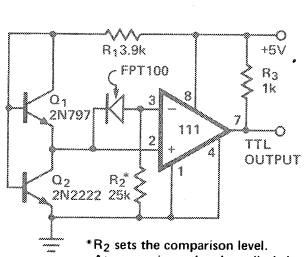
DIGITAL TRANSMISSION ISOLATOR



STROBING OF BOTH INPUT AND OUTPUT STAGES

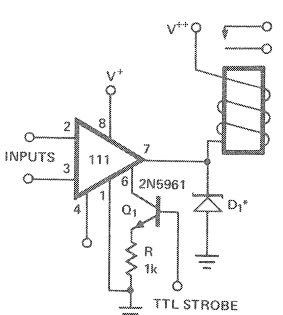


PRECISION PHOTODIODE COMPARATOR



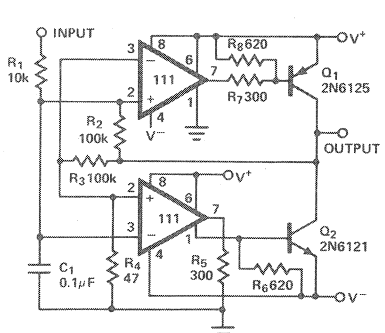
*R_2 sets the comparison level. At comparison, the photodiode has less than 5mV across it, decreasing leakages by an order of magnitude.

RELAY DRIVER WITH STROBE



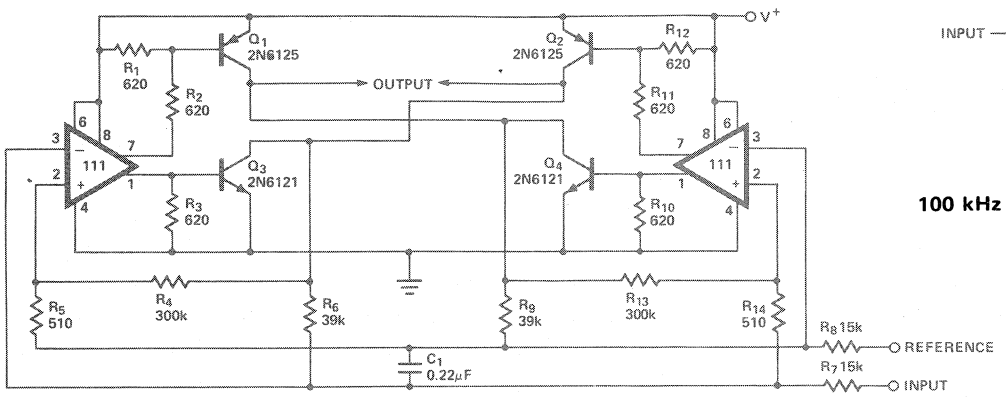
*Absorbs inductive kickback of relay and protects IC from voltage transients.

SWITCHING POWER AMPLIFIER

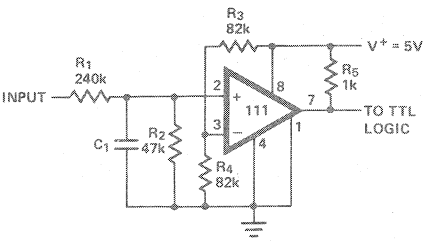


Typical Applications (Cont'd.)

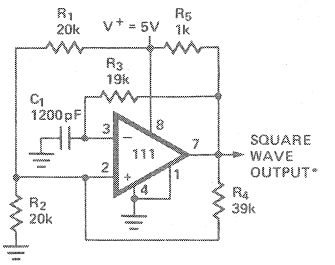
SWITCHING POWER AMPLIFIER



TTL INTERFACE WITH HIGH LEVEL LOGIC



100 kHz FREE RUNNING MULTIVIBRATOR



139 Series

139•239•339•139A•239A•339A

Quad Comparators

Features

- WIDE SUPPLY VOLTAGE RANGE – +2 TO +36 VDC (SINGLE SUPPLY), ±1 TO ±18 VDC (DUAL)
- LOW SUPPLY CURRENT DRAIN – 0.8 mA
- LOW INPUT BIASING CURRENT – 35 nA
- LOW INPUT OFFSET CURRENT AND VOLTAGE – 3 nA, 3 mV
- LOW OUTPUT SATURATION VOLTAGE – 1 mV AT 5 μA, 70 mV AT 1 mA
- OUTPUT VOLTAGE COMPATIBLE WITH ALL LOGIC FAMILIES

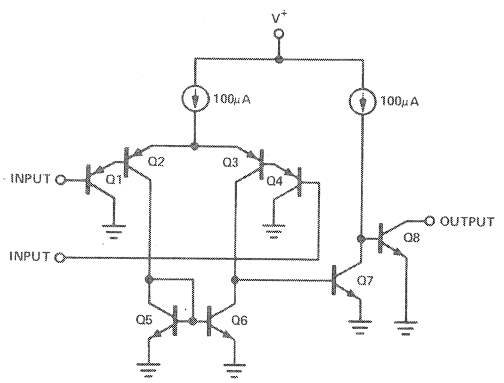
Description

The Teledyne 139 series consists of four independent voltage comparators designed to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible, and the low power supply current drain is independent of the magnitude of the power supply voltage. The input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The 139 series was designed to interface directly with TTL and CMOS. When operated from both plus and minus power supplies, the 339 will interface directly with MOS logic, where the low power drain of the 339 is a distinct advantage over standard comparators.

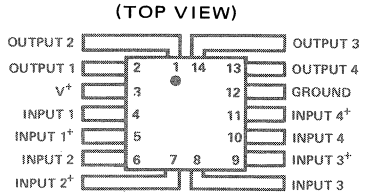
The 139/139A is designed to operate over a temperature range of −55°C to +125°C. The 239/239A operates from −25°C to +85°C. For operation over a 0°C to +70°C temperature range use the 339/339A.

Equivalent Circuit Diagram

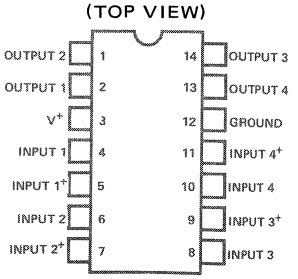


Connection Diagrams

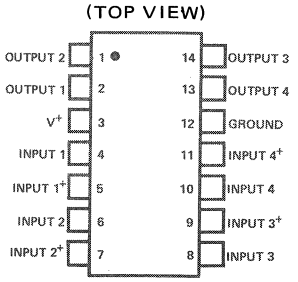
H PACKAGE
14 LEAD FLATPACK
(TOP VIEW)



L PACKAGE
14 LEAD CERDIP
(TOP VIEW)



J PACKAGE
14 LEAD PLASTIC DIP
(TOP VIEW)



H, L AND J PACKAGES

Order Part Numbers:

Flat Pack	LM139F, LM139AF
Cer DIP	LM139D, LM139AD LM239D, LM239AD LM339D, LM339AD
Plastic DIP	LM339N, LM339AN

Absolute Maximum Ratings

Differential Input Voltage	36 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}
Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}
Power Dissipation (Note 1)	
Molded DIP	570 mW
Cavity DIP	900 mW
Flatpack	800 mW
Output Short-Circuit to GND (Note 2)	Continuous
Operating Temperature Range	
339	0°C to +70°C
239	−25°C to +85°C
139	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (V^+ = +5V, T_A = 25°C)

PARAMETER	CONDITIONS	139			239, 339			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage 139, 239, 339 139A, 239A, 339A	$V_O \cong 1.4V_{DC}$, V_{REF} = $1.4V_{DC}$, $R_S = 0\Omega$		2 1	5 2		2 1	5 2	mV mV
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$		3	25		5	50	nA
Input Bias Current [3]	Output In Linear Range		25	100		25	250	nA
Input Common-Mode Voltage Range [4]		0		V^+ −1.5	0		V^+ −1.5	V_{DC}
Supply Current	$R_L = \infty$ On All Comparators		.8	2		.8	2	mA
Voltage Gain	R_L = 15KΩ		200			200		V/mV
Propagation Delay Time	100mV Input Step With 5mV Overdrive V_{RL} = 5.0 VDC, R_L = 5.1 kΩ		1.3			1.3		μsec
Output Sink Current	$V_{OL} \leq 1.5V_{DC}$	6	16		6	16		mA
Low Level Output Voltage	I_{SINK} = 3mA		.25	.5		.25	.5	V_{DC}
Output Leakage Current	(Output Voltage High)		.1			.1		nA
The Following Specifications Apply For:		−55°C to +125°C			0°C to +70°C 339 −25°C to +85°C 239			
Input Offset Voltage	$V_O \cong 1.4V_{DC}$ $V_{REF} = 1.4V_{DC}$ $R_S = 0\Omega$			9.0			9.0	mV
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			100			150	nA
Input Bias Current	Output in Linear Range			300			400	nA
Input Common-Mode Voltage		0		V^+ −2.0	0		V^+ −2.0	V_{DC}
Saturation Voltage	$I_{SINK} \leq 4.0$mA			700			700	mV
Output Leakage Current	V_{OUT} = 30V			1.0			1.0	μA
Differential Input Voltage	$V_{IN'S} > 0V_{DC}$			36			36	V_{DC}

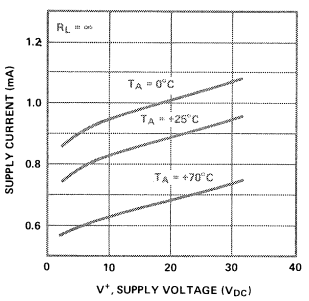
Electrical Characteristics (Cont'd.)

NOTES:

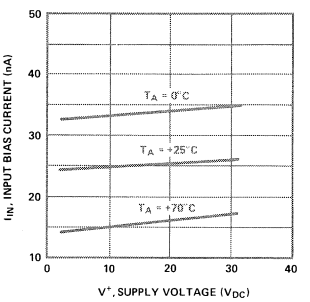
1. For operating at high temperatures, the 339 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The 239 and 139 must be derated based on a +150°C maximum junction temperature. The low bias dissipation and the ON-OFF characteristic of the outputs keeps the chip dissipation very small (Pd ≤ 100 mW), provided the output transistors are allowed to saturate.
2. Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
4. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+ –1.5V, but either or both inputs can go to +30V_{DC} without damage.

Typical Characteristics

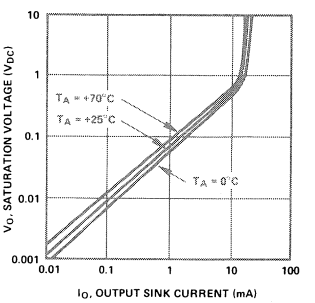
SUPPLY CURRENT



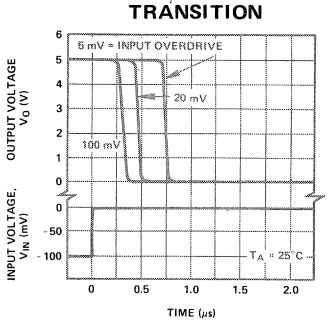
INPUT CURRENT



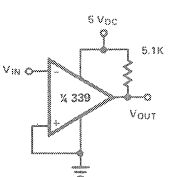
OUTPUT SATURATION VOLTAGE



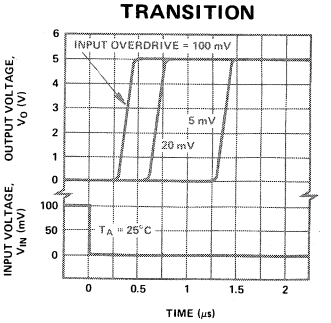
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES – NEGATIVE TRANSITION



RESPONSE TIME TEST SCHEMATIC

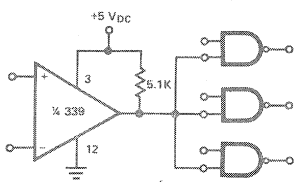


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES – POSITIVE TRANSITION

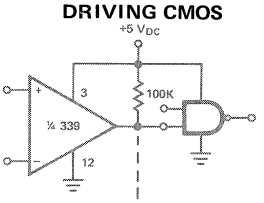


Typical Applications (See also 3302)

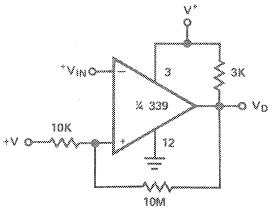
DRIVING TTL



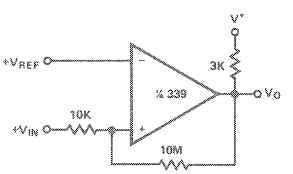
DRIVING CMOS



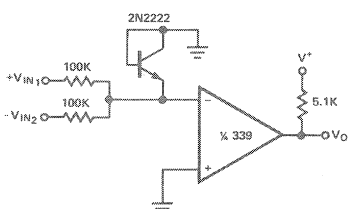
COMPARATOR WITH HYSTERESIS



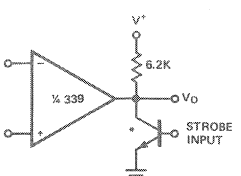
NON-INVERTING COMPARATOR WITH HYSTERESIS



COMPARING INPUT VOLTAGES OF OPPOSITE POLARITY

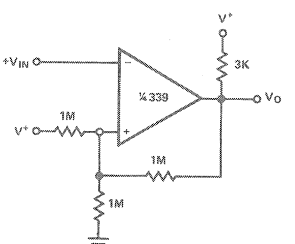


OUTPUT STROBING

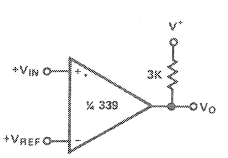


*OR LOGIC GATE WITHOUT PULL-UP RESISTOR

INVERTING COMPARATOR WITH HYSTERESIS



BASIC COMPARATOR



710
Differential Comparators

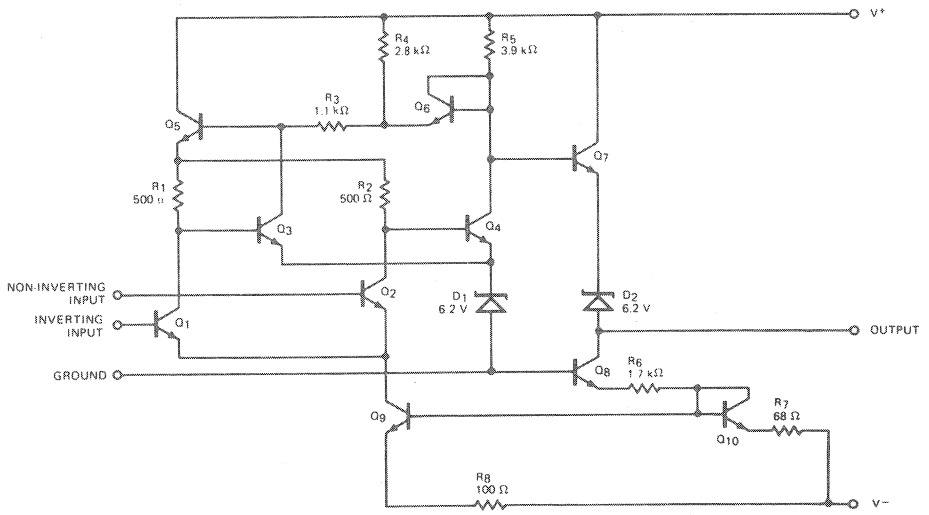
Features

- 5mV MAXIMUM OFFSET VOLTAGE
- 5μA MAXIMUM OFFSET CURRENT
- 1000 MINIMUM VOLTAGE GAIN
- 20μV/°C MAXIMUM OFFSET VOLTAGE DRIFT

Description

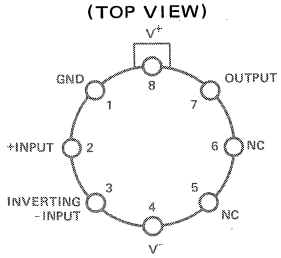
The Teledyne 710 differential voltage comparator is intended for applications requiring high accuracy and fast response times. It features both inverting and non-inverting inputs and a TTL compatible output. Applications include variable threshold Schmitt triggers, pulse height discriminators, A to D converters, memory sense amplifiers, and high noise immunity line receivers. The 710B is intended for operation over the full military temperature range from −55°C to +125°C. The 710C, commercial equivalent of the 710B, will operate over a temperature from 0°C to +70°C.

Equivalent Circuit Diagram



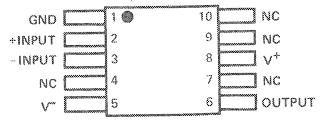
Connection Diagrams

E PACKAGE
8 LEAD METAL CAN
(TOP VIEW)



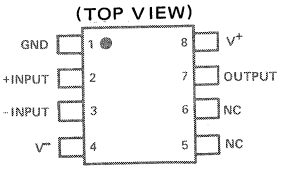
Order Part Numbers:
710BE, 710CE

H PACKAGE
10 LEAD FLATPACK
(TOP VIEW)



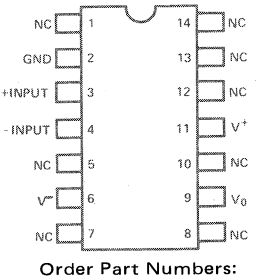
Order Part Number:
710BH

P PACKAGE
8 LEAD MINIDIP
(TOP VIEW)



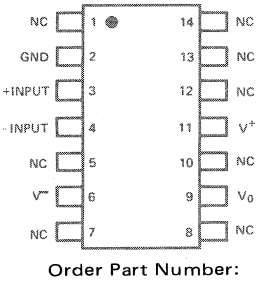
Order Part Number:
710CP

L PACKAGE
14 LEAD CERDIP
(TOP VIEW)



Order Part Numbers:
710BL, 710CL

J PACKAGE
14 LEAD PLASTIC DIP
(TOP VIEW)



Order Part Number:
710CJ

Absolute Maximum Ratings

	710B	710C
Differential Input Voltage	±5.0V	±5.0V
Input Voltage (Note 1)	±7.0V	±7.0V
Peak Output Current	10mA	10mA
Output Short Circuit Duration (Note 2)	Indefinite	Indefinite
Positive Supply Voltage	+14.0V	+14.0V
Negative Supply Voltage	−7.0V	−7.0V
Internal Power Dissipation (Note 3)		
Metal Can (E)	500mW	500mW
Ceramic Dual-In-Line (N)	670mW	670mW
Plastic Dual-In-Line (J)	NA	530mW
Flatpack (H)	570mW	570mW
Storage Temperature Range	−65°C/+150°C	−65°C/+150°C
Operating Temperature Range	−55°C/+125°C	0°C/+70°C
Lead Soldering Temperature (60 sec)	300°C	300°C
Junction Temperature	150°C	150°C

The above ratings are not meant to imply operation at each of these extremes simultaneously. Exceeding any or all of the absolute maximum ratings may cause permanent damage to the device.

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
3. Rating applies to ambient temperature up to 75°C ambient. For operation above T_A = 75°C, derate linearly 6.7 mW/°C for the metal can, 8.9 mW/°C for the ceramic dual-in-line, and 7.5 mW/°C for the flatpack. For the flatpack, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16" thick, epoxy-glass board with ten 0.03"-wide, 2 oz. copper conductors.

Electrical Characteristics (T_A = 25°C, V+ = 12V, V− = −6.0V unless otherwise specified)

PARAMETER	CONDITIONS	710B			710C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (Note 1)	$R_S \leq 200\Omega$		0.6	2.0		1.6	5.0	mV
Input Offset Current (Note 1)			0.75	3.0		1.8	5.0	μA
Input Bias Current			13	20		16	25	μA
Voltage Gain		1250	1700		1000	1500		
Output Resistance			200			200		Ω
Output Sink Current	$\Delta V_{IN} \geq 5mV$, V_{OUT} = 0	2.0	2.5		1.6	2.5		mA
Response Time (Note 2)			40			40		ns
The Following Specifications Apply Over the Operating Temperature Ranges:								
Input Offset Voltage	$R_S \leq 200\Omega$			3.0			6.5	mV
Average Temperature Coefficient of Input Offset Voltage, 710B	R_S = 50Ω, T_A = 25°C to +125°C T_A = 25°C to −55°C		3.5 2.7	10 10				μV/°C
Average Temperature Coefficient of Input Offset Voltage, 710C	R_S = 50Ω, T_A = 0°C to 70°C					5.0	20	μV/°C
Input Offset Current, 710B	T_A = +125°C T_A = −55°C		 1.8	3.0 7.0				μA
Input Offset Current, 710C							7.5	μA
Average Temperature Coefficient of Input Offset Current, 710B	T_A = 25°C to +125°C T_A = 25°C to −55°C		5.0 15	25 75				nA/°C
Average Temperature Coefficient of Input Offset Current, 710C	T_A = 25°C to +70°C T_A = 25°C to 0°C					15 24	50 100	nA/°C
Input Bias Current	T_A = −55°C (710B); T_A = 0°C (710C)		27	45		25	40	μA
Input Voltage Range	V− = −7.0V	±5.0			±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\Omega$	80	100		70	98		dB
Differential Input Voltage Range		±5.0			±5.0			V
Voltage Gain		1000			800			
Output HIGH Voltage	$\Delta V_{IN} \geq 5mV$, $0 \leq I_{OUT} \leq 5.0mA$	2.5	3.2	4.0	2.5	3.2	4.0	V
Output LOW Voltage	$\Delta V_{IN} \geq 5mV$	−1.0	−0.5	0	−1.0	−0.5	0	V
Output SINK Current, 710B	$\Delta V_{IN} \geq 5mV$, V_{OUT} = 0, T_A = +125°C T_A = −55°C	0.5 1.0	1.7 2.3					mA
Output SINK Current, 710C	$\Delta V_{IN} \geq 5mV$, V_{OUT} = 0				0.5			mA
Positive Supply Current	$V_{OUT} \leq 0$		5.2	9.0		5.2	9.0	mA
Negative Supply Current	V_{OUT} = Gnd, Inverting Input = +5mV		4.6	7.0		4.6	7.0	mA
Power Consumption	V_{OUT} = Gnd, Inverting Input = +10mV		90	150		90	150	mW

NOTES:
1. The input offset voltage and input offset current are specified for a logic threshold voltage as follows: for 710B, 1.8V at −55°C, 1.4V at +25°C, 1.0V at +125°C; for 710C, 1.5V at 0°C, 1.4V at +25°C, and 1.2V at +70°C.
2. The response time specified is for a 100mV input step with 5mV overdrive.

711
Dual Differential Comparators

Features

- FAST RESPONSE TIME . . . 40ns TYPICAL
- 5mV MAXIMUM OFFSET VOLTAGE
- 10μA MAXIMUM OFFSET CURRENT
- INDEPENDENT STROBING OF EACH COMPARATOR

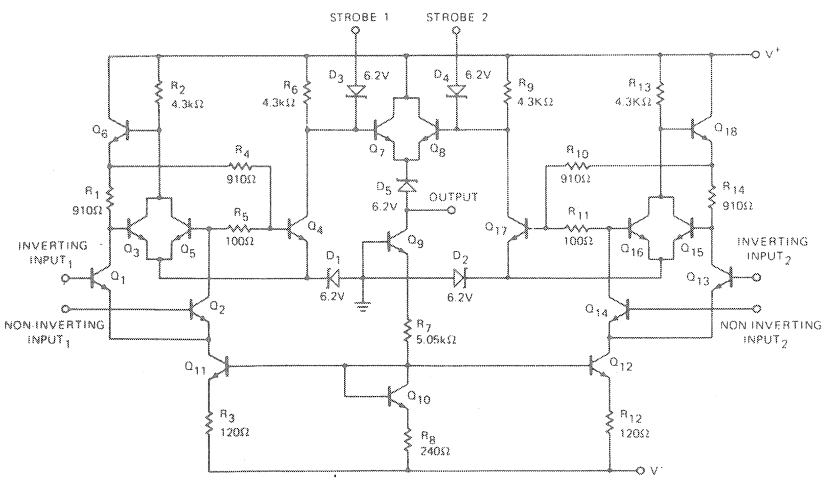
Description

The Teledyne Semiconductor 711 is a dual differential voltage comparator for use in core-memory sense applications. Its TTL compatible output, high accuracy, fast response times, and large input voltage range make it also useful as a window discriminator in pulse height detectors. In addition, the 711 can be used in double-ended limit detectors for automatic Go/No-Go test equipment.

Its very flexible design provides easy adjustment of the threshold voltage over a wide range, independent strobing of the comparator channels, and even pulse stretching on the output.

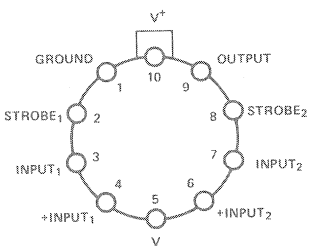
The 711B operates over the full military temperature range from −55°C to +125°C. The 711C operates over a temperature range from 0°C to +70°C.

Equivalent Circuit Diagram



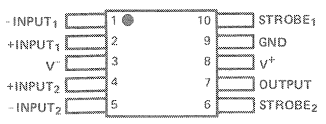
Connection Diagrams

E PACKAGE
10 LEAD METAL CAN
(TOP VIEW)



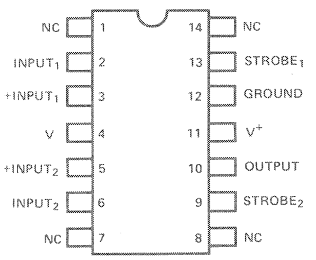
Order Part Numbers:
711BE, 711CE

H PACKAGE
10 LEAD FLATPACK
(TOP VIEW)



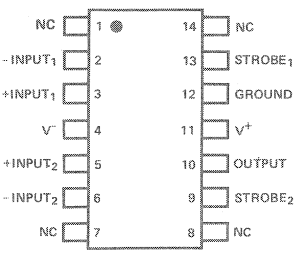
Order Part Number:
711BH

L PACKAGE
14 LEAD CERDIP
(TOP VIEW)



Order Part Numbers:
711BL, 711CL,

J PACKAGE
14 LEAD PLASTIC DIP
(TOP VIEW)



Order Part Number:
711CJ

Absolute Maximum Ratings

	711B	711C
Differential Input Voltage	±5.0V	±5.0V
Input Voltage (Note 1)	±7.0V	±7.0V
Peak Output Current	50mA	50mA
Output Short Circuit Duration (Note 2)	Indefinite	Indefinite
Positive Supply Voltage	+14V	+14V
Negative Supply Voltage	−7.0V	−7.0V
Strobe Voltage	0 to +6.0V	0 to +6.0V
Internal Power Dissipation (Note 3)		
Metal Can (E)	500mW	500mW
Ceramic Dual-In-Line (N)	670mW	670mW
Plastic Dual-In-Line (J)	NA	530mW
Flatpack (H)	570mW	570mW
Storage Temperature Range	−65°C/+150°C	−65°C/+150°C
Operating Temperature Range	−55°C/+125°C	0°C/+70°C
Lead Soldering Temperature (60 sec)	300°C	300°C
Junction Temperature	150°C	150°C

The above ratings are not meant to imply operation at each of these extremes simultaneously. Exceeding any or all of the absolute maximum ratings may cause permanent damage to the device.

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
3. Rating applies to ambient temperature up to 75°C ambient. For operation above T_A = 75°C, derate linearly 6.7mW/°C for the metal can, 8.9mW/°C for the ceramic dual-in-line, and 7.5mW/°C for the flatpack. For the flatpack, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16" thick, epoxy-glass board with ten 0.03" wide, 2 oz. copper conductors.

Electrical Characteristics (T_A = 25°C, V+ = 12V, V− = −6.0V unless otherwise specified)

PARAMETER	CONDITIONS	711B			711C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	V_{OUT} = +1.4V, $R_S \leq 200\Omega$, V_{CM} = 0		1.0	3.5		1.0	5.0	mV
	V_{OUT} = +1.4V, $R_S \leq 200\Omega$		1.0	5.0		1.0	7.5	mV
Input Offset Current	V_{OUT} = 1.4V		0.5	10.0		0.5	15	μA
Input Bias Current			25	75		15	100	μA
Voltage Gain		750	1500		700	1500		
Response Time (Note 1)			40			40		ns
Strobe Release Time			12			12		ns
Input Voltage Range	V− = −7.0V	±5.0			±5.0			V
Differential Input Voltage Range		±5.0			±5.0			V
Output Resistance			200			200		Ω
Output HIGH Voltage	$V_{IN} \geq 10mV$		4.5	5.0		4.5	5.0	V
Loaded Output HIGH Voltage	$V_{IN} \geq 10mV$, I_O = 5mA	2.5	3.5		2.5	3.5		V
Output LOW Voltage	$V_{IN} \geq 10mV$	−1.0	−0.5	0	−1.0	−0.5	0	V
Strobed Output Level	$V_{STROBE} \leq 0.3V$	−1.0		0	−1.0		0	V
Output Sink Current	$V_{IN} \geq 10mV$, $V_{OUT} \geq 0$	0.5	0.8		0.5	0.8		mA
Strobe Current	V_{STROBE} = 100mV		1.2	2.5		1.2	2.5	mA
Positive Supply Current	V_{OUT} = Gnd, Inverting Input = +5mV		8.6			8.6		mA
Negative Supply Current	V_{OUT} = Gnd, Inverting Input = +5mV		3.9			3.9		mA
Power Consumption			130	200		130	230	mW

Electrical Characteristics (Cont'd.)

The Following Specifications Apply Over the Operating Temperature Ranges:

PARAMETER	CONDITIONS	711B			711C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage (Note 2)	$R_S \leqslant 200\Omega$, $V_{CM} = 0$ $R_S \leqslant 200\Omega$			4.5 6.0			6.0 10	mV mV
Input Offset Current (Note 2)				20			25	μA
Input Bias Current				150			150	μA
Temperature Coefficient of Input Offset Voltage			5.0			5.0		μV/°C
Voltage Gain		500			500			

NOTES: 1. The response time specified is for a 100mV step input with 5mV overdrive.

2. The input offset voltage is specified for a logic threshold as follows: for the 711B, 1.8V at −55°C, 1.4V at +25°C, 1.0V at +125°C; for 711C, 1.5V at 0°C, 1.4V at +25°C, 1.2V at +70°C.

2901
Quad Differential Comparator

Features

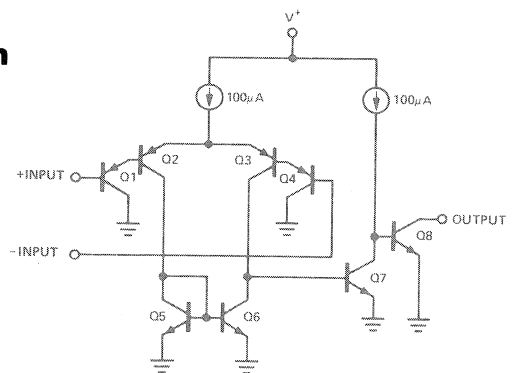
- WIDE SINGLE SUPPLY VOLTAGE RANGE – ($2V_{DC}$ TO $36V_{DC}$) OR DUAL SUPPLIES ($\pm 1V_{DC}$ TO $\pm 18V_{DC}$)
- VERY LOW SUPPLY CURRENT DRAIN (0.8mA) – INDEPENDENT OF SUPPLY VOLTAGE (1mW/ COMPARATOR AT $+5V_{DC}$)
- LOW INPUT BIASING CURRENT (35nA)
- LOW INPUT OFFSET CURRENT (3nA) AND OFFSET VOLTAGE (3mV)
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO POWER SUPPLY VOLTAGE
- LOW OUTPUT SATURATION VOLTAGE (1mV AT 5μA, 70mV AT 1mA)
- OUTPUT VOLTAGE COMPATIBLE WITH TTL (FANOUT OF 3), DTL, ECL, MOS AND CMOS LOGIC SYSTEMS

Description

The Teledyne Semiconductor 2901 consists of four independent voltage comparators designed specifically to operate over a temperature range from –40°C to +85°C and from a single power supply over a wide range of voltages. Operation from split power supplies is also possible, and the low power supply current drain is independent of the magnitude of the power supply voltage. The input common-mode voltage range includes ground, even though operated from a single power supply voltage.

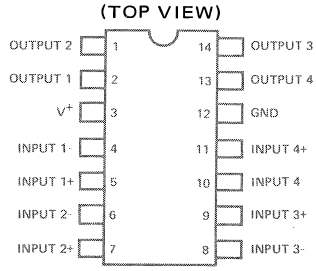
Applications include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. When operated from both plus and minus power supplies, the 2901 will directly interface with MOS logic – where the low power drain of the 2901 is a distinct advantage over standard comparators.

Equivalent Circuit Diagram



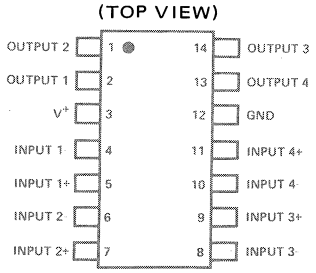
Connection Diagrams

L PACKAGE
14 LEAD CERDIP
(TOP VIEW)



Order Part Numbers:
LM2901N, LM2901L

J PACKAGE
14 LEAD PLASTIC DIP
(TOP VIEW)



Order Part Number:
LM2901N

Absolute Maximum Ratings

Differential Input Voltage	$36V_{DC}$
Input Voltage	$-0.3V_{DC}$ to $+36V_{DC}$
Output Short-Circuit to GND (Note 1)	Continuous
Supply Voltage, V^+	$36V_{DC}$ or $\pm 18V_{DC}$
Power Dissipation (Note 2)	570mW
Operating Temperature Range	$-40°C/+85°C$
Storage Temperature Range	$-65°C/+150°C$
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics ($V^+ = 5V$, $T_A = 25°C$)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	At Output Switch Point, $V_O \cong 1.4V_{DC}$, $V_{REF} = +1.4V_{DC}$ and $R_S = 0\Omega$		2	5	mV_{DC}
Input Bias Current (Note 3)	$I_{IN(+)}$ or $I_{IN(-)}$ With Output in Linear Range		25	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$		5	50	nA_{DC}
Input Common-Mode Voltage Range (Note 4)		0		$V^+ - 1.5$	V_{DC}
Supply Current	$R_L = \infty$ On All Comparators		0.8	2	mA_{DC}
Voltage Gain	$R_L = 15K\Omega$		200		V/mV
Response Time (Note 5)	$V_{RL} = 5.0V_{DC}$ and $R_L = 5.1K\Omega$		1.3		μs
Output Sink Current	$V_{IN(-)} = +1V_{DC}$, $V_{IN(+)} = 0$ and $V_O \leqslant +1.5V_{DC}$	6	16		mA_{DC}
Saturation Voltage	$V_{IN(-)} = +1V_{DC}$, $V_{IN(+)} = 0$ and $I_{SINK} = 3mA$		200	400	mV_{DC}
Output Leakage Current	$V_{IN(+)} = +1V_{DC}$, $V_{IN(-)} = 0$ and $V_{OUT} = 5V_{DC}$		0.1		nA_{DC}

NOTES:

1. Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V^+.
2. For operating at high temperatures, the 2901 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The low bias dissipation and the ON-OFF characteristic of the outputs keeps the chip dissipation very small ($P_d \leqslant 100mW$), provided the output transistors are allowed to saturate.
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
4. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to $+30V_{DC}$ without damage.
5. The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300ns can be obtained, see typical performance characteristics section.

3302
Quad Differential Comparator

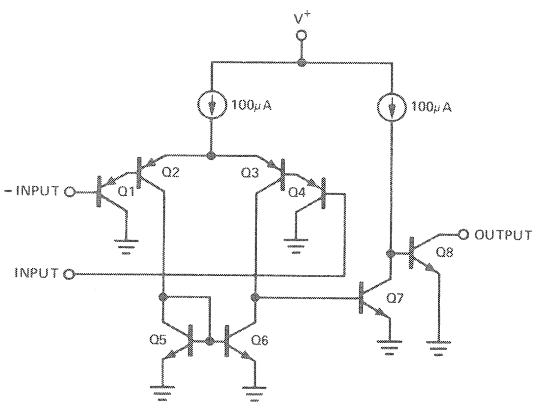
Features

- WIDE OPERATING TEMPERATURE RANGE – −40 TO +85°C
- SINGLE-SUPPLY OPERATION – +2.0 to +28 Vdc
- DIFFERENTIAL INPUT VOLTAGE = $\pm V_{CC}$
- COMPARE VOLTAGES AT GROUND POTENTIAL
- TTL COMPATIBLE
- LOW CURRENT DRAIN – 700μA @ V_{CC} = 5.0 Vdc
- OUTPUTS CAN BE CONNECTED TO GIVE THE IMPLIED AND FUNCTION

Description

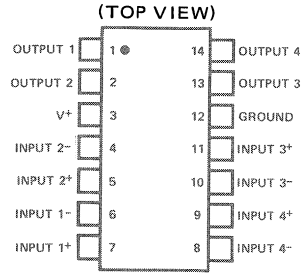
The Teledyne 3302 contains four independent comparators, planar epitaxially constructed on a single monolithic chip. Designed specifically for single positive power supply operation, the 3302 has wide application in consumer and industrial electronics.

Equivalent Circuit Diagram



Connection Diagram

J PACKAGE
14 LEAD PLASTIC DIP
(TOP VIEW)



Order Part Number:
3302J

Absolute Maximum Ratings (T_A = +25°C unless otherwise noted.)

RATING	SYMBOL	VALUE	UNIT
Power Supply Range	V_{CC}	+2.0 to +28	Vdc
Output Sink Current[1]	I_O	20	mA
Differential Input Voltage	V_{IDR}	$\pm V_{CC}$	Vdc
Common-Mode Input Voltage Range[2]	V_{ICR}	−0.3 to $+V_{CC}$	Vdc
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	625 5.0	mW mW/°C
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTES:

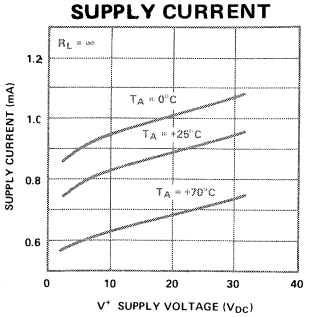
1. Requires an external resistor, R_L, to limit current below maximum rating.
2. If either (+) or (−) inputs of any comparator go more than several tenths of a volt below ground, a parasitic transistor turns "on" causing high input current and possible faulty outputs.

Electrical Characteristics (V_{CC} = +15 Vdc, T_A = +25°C (each comparator) unless otherwise noted.)

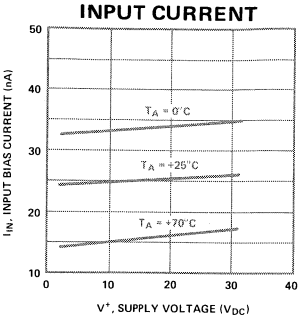
CHARACTERISTIC	FIGURE	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage (V_{ref} = 1.2 Vdc) (T_A = +25°C) (T_A = −40 to +85°C)	1	V_{IO}	 − −	 3.0 −	 20 40	mVdc
Input Offset Current		I_{IO}	−	3.0	−	nAdc
Input Bias Current (T_A = +25°C) (T_A = −40 to +85°C)		I_{IB}	 − −	 30 −	 500 1,000	nAdc
Voltage Gain (T_A = +25°C, R_L = 15kΩ)	2	A_{vol}	 2,000	 30,000	 −	V/V
Transconductance		gm	−	2.0	−	mhos
Differential Input Voltage Range		V_{IDR}	$\pm V_{CC}$	−	−	Vdc
Output Leakage Current (Output Voltage High)	3	I_{off}	 −	 −	 1.0	μAdc
Negative Output Voltage (I_S = 2.0mA, V_{CC} = +5.0 to +28 Vdc)		V_{OL}	 −	 150	 400	mVdc
Output Sink Current (V_{CC} = +5.0 Vdc) (T_A = +25°C, V_{OL} = 400mV) (T_A = −40 to +85°C, V_{OL} = 800mV)		I_S	 − 2.0	 6.0 −	 − −	mAdc
Input Common-Mode Range (V_{CC} = +28 Vdc)	4	V_{ICR}	 0-26	 −	 −	Volts
Common-Mode Rejection Ratio		CMRR	−	60	−	dB
Propagation Delay Time For Positive and Negative-Going Input Pulse	5	$t_{PHL/LH}$	 −	 2.0	 −	μs
Slew Rate (R_L = 15kΩ)		t_{SR^-} t_{SR^+}	 − −	 200 50	 − −	V/μs
Power Supply Current (Total of four comparators) (I_S = 0, V_{CC} = +5.0 to +28 Vdc)	6	I_D	 −	 0.7	 1.5	mAdc

Typical Characteristics

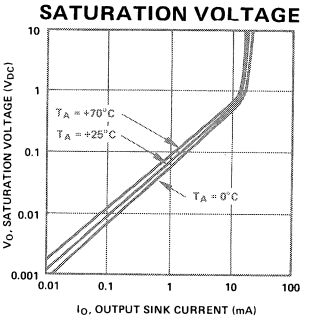
SUPPLY CURRENT



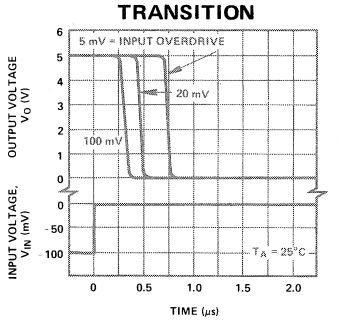
INPUT CURRENT



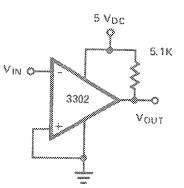
OUTPUT SATURATION VOLTAGE



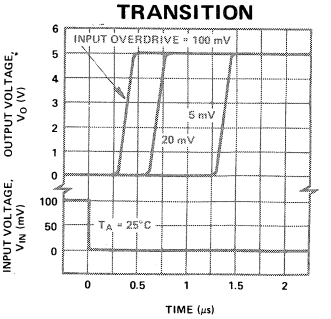
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES – NEGATIVE TRANSITION



RESPONSE TIME TEST SCHEMATIC



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES – POSITIVE TRANSITION



Test Circuits (1/4 Circuit Shown)

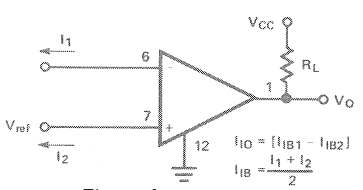


Figure 1

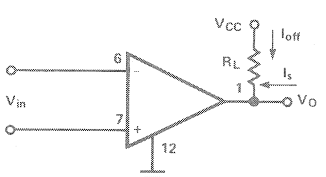


Figure 3

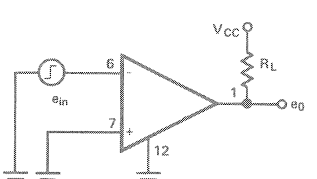
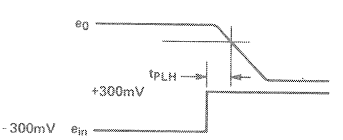


Figure 5



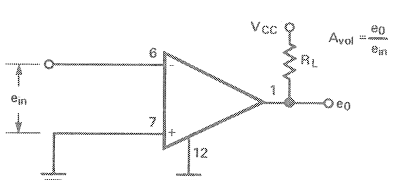


Figure 2

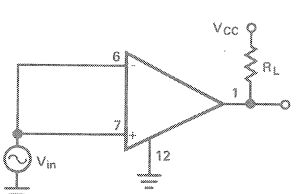


Figure 4

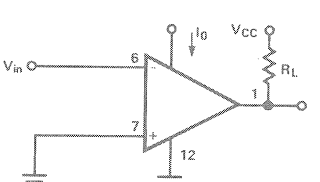
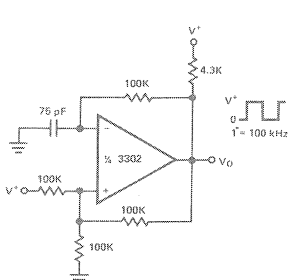


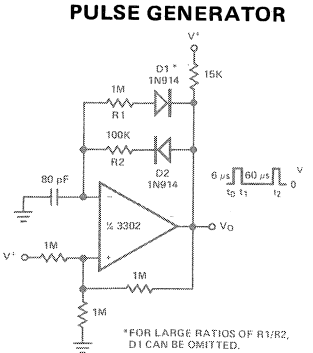
Figure 6

Typical Applications (See also 139 Series)

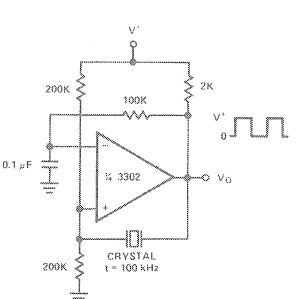
SQUAREWAVE OSCILLATOR



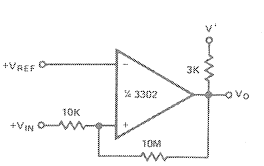
PULSE GENERATOR



CRYSTAL CONTROLLED OSCILLATOR



NON-INVERTING COMPARATOR WITH HYSTERESIS



75450/75460 Series

Including 75450B Series

Dual Peripheral Drivers

Features

- HIGH SPEED SWITCHING
- HIGH OUTPUT CURRENT CAPABILITY
- UNCOMMITTED COLLECTOR OUTPUT DEVICES FOR HIGH OUTPUT VOLTAGE CAPABILITY
- TTL OR DTL INPUT COMPATIBILITY
- INPUT CLAMP DIODES
- +5 VOLT SUPPLY VOLTAGE

Summary — 75450/75460 SERIES DUAL DRIVERS

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGE
75450/75450B/75460	AND†	14 pin silicon DIP
75451/75451B/75461	AND	8 pin MINI-DIP
75452/75452B/75462	NAND	8 pin MINI-DIP
75453/75453B/75463	OR	8 pin MINI-DIP
75454/75454B/75464	NOR	8 pin MINI-DIP

†With transistor base connected externally to output of gate.

Description

Teledyne Semiconductor's 75450, 75450B, and 75460 Series are dual general purpose interface drivers that convert TTL and DTL logic levels to high current, high voltage drive capability. The 75450 features two TTL NAND gates and two uncommitted transistors. The 75451, 75452, 75453 and 75454 feature two standard series 74 TTL gates in AND, NAND, OR and NOR configurations respectively, driving the base of two high voltage, high current, uncommitted collector output transistors.

Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, line drivers, MOS drivers, and memory drivers. The Teledyne 75450 and 75451 are functionally interchangeable with SN75450/75450A and SN75451/75451A, respectively.

The 75460 series is pin interchangeable with the 75450 series and are recommended for use in applications requiring a minimum collector to emitter breakdown voltage of 60V.

The 75450B series is functionally interchangeable with industry standard 75450 and 75450A series, but has more tightly controlled switching parameters for critical applications. A test to ensure freedom from latch-up also has been added.

Absolute Maximum Ratings

	75450/75450B	75460	75451/75451B 75452/75452B 75453/75453B 75454/75454B	75461 75462 75463 75464
Input Voltage(1)	5.5V	5.5V	5.5V	5.5V
Output Voltage(1) (4)			30V	60V
Continuous Output Current(5)			300mA	300mA
Supply Voltage, V_{CC}	7V	7V	7V	7V
Interemitter Voltage(2)	5.5V	5.5V	5.5V	5.5V
V_{CC} to Substrate Voltage(6)	35V	40V		
Collector to Substrate Voltage(6)	35V	40V		
Collector-base Voltage	35V	40V		
Collector-emitter Voltage(3)	30V	40V		
Emitter-base Voltage	5V	5V	5V	5V

Absolute Maximum Ratings (Cont'd.)

	75450/75450B/75460	75451/75451B/75461 75452/75452B/75462 75453/75453B/75463 75454/75454B/75464
Continuous Collector Current[5]	300mA	300mA
Continuous Total Power Dissipation[7]	800mW	800mW
Operating Free-Air Temperature Range	0°C to 70°C	0°C to 70°C
Storage Temperature Range Molded DIP	−55°C to 125°C	−55°C to 125°C
Lead Temperature Molded DIP (Soldering, 10 seconds) Hermetic DIP (Soldering, 30 seconds)	 260°C 300°C	 260°C 300°C

NOTES:

1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter input transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual circuits may conduct rated current simultaneously.
6. For the 75450, 75450B and 75460 only, the substrate (Pin 8) must always be at the most negative device voltage for proper operation.
7. Above 50°C ambient temperature, derate linearly at 8.3mW/°C.

Test Circuits (Arrows indicate direction of current flow. Current into terminal is a positive value.)

Fig. 1. V_{IH}, V_{OL}
Both inputs are tested simultaneously.

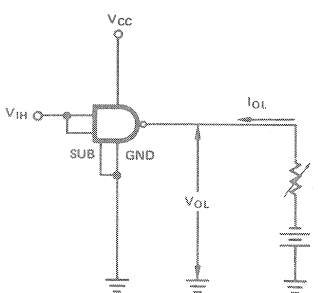


Fig. 2. V_{IL}, V_{OH}
Each input is tested separately.

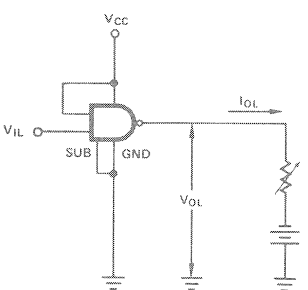


Fig. 3. V_I, I_{IL}
Each input is tested separately.

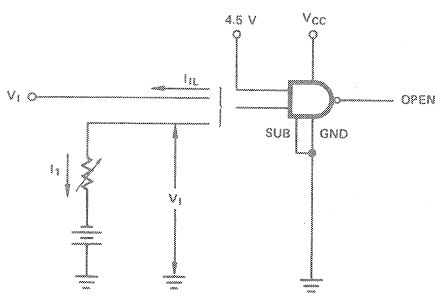


Fig. 4. I_I, I_{IH}
Each input is tested separately.

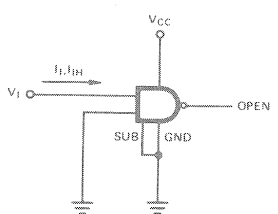


Fig. 5. I_{OS}
Each gate is tested separately.
(75450, 75450B, and 75460 only.)

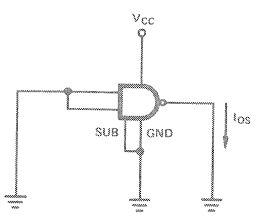
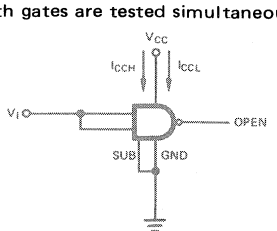
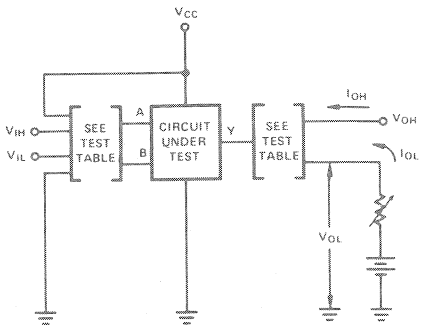


Fig. 6. I_{CCH}, I_{CCL}
Both gates are tested simultaneously.



Test Circuits (Cont'd.)

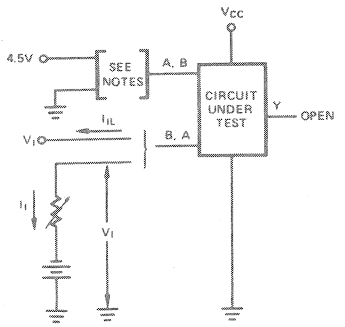
Fig. 7. V_{IH}, V_{IL}, I_{OH}, V_{OL}
Each input is tested separately.



CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
75451,B	V_{IH}	V_{IH}	V_{OH}	I_{OH}
75461	V_{IL}	V_{CC}	I_{OL}	V_{OL}
75452,B	V_{IH}	V_{IH}	I_{OL}	V_{OL}
75462	V_{IL}	V_{CC}	V_{OH}	I_{OH}
75453,B	V_{IH}	GND	V_{OH}	I_{OH}
75463	V_{IL}	V_{IL}	I_{OL}	V_{OL}
75454,B	V_{IH}	GND	I_{OL}	V_{OL}
75464	V_{IL}	V_{IL}	V_{OH}	I_{OH}

NOTE: Each input is tested separately.

Fig. 8. V_I, I_{IL}

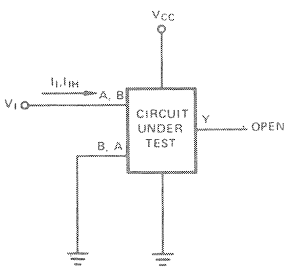


NOTES:

A. Each input is tested separately.

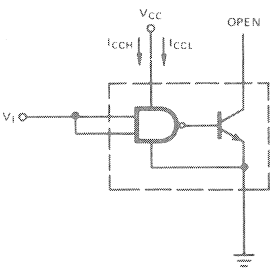
B. When testing 75453, B/75463 and 75454, B/75464, input not under test is grounded. For all other circuits it is at 4.5V.

Fig. 9. I_I, I_{IH}



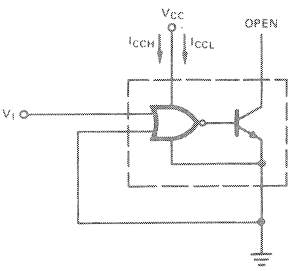
Each input is tested separately.

Fig. 10. I_{CCH}, I_{CCL}
For AND, NAND Circuits



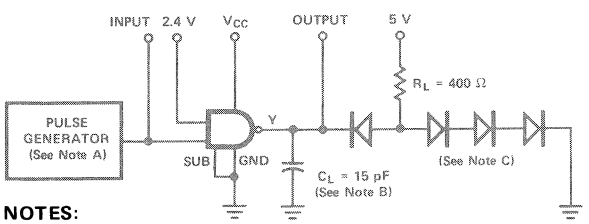
Both gates are tested simultaneously.

Fig. 11. I_{CCH}, I_{CCL}
For OR, NOR Circuits



Both gates are tested simultaneously.

Fig. 12. PROPAGATION DELAY TIMES, EACH GATE
(75450, 75460 ONLY)

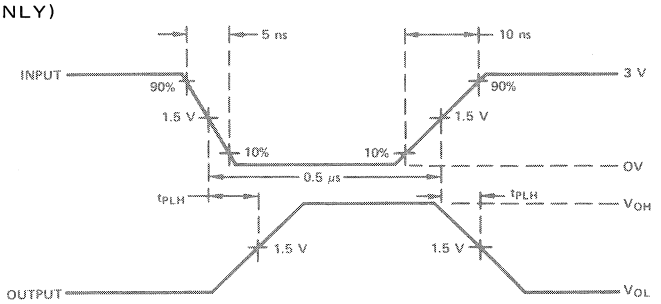


NOTES:

A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.

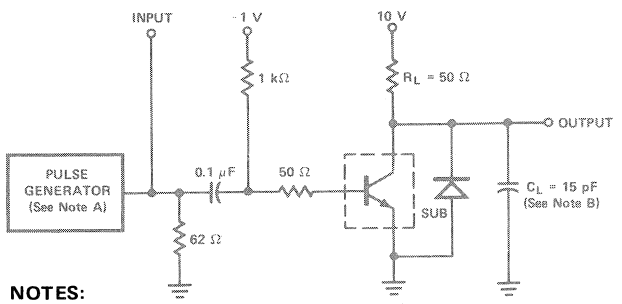
B. C_L include probe and jig capacitance.

C. All diodes are 1N3064 or equivalent.



VOLTAGE WAVEFORMS

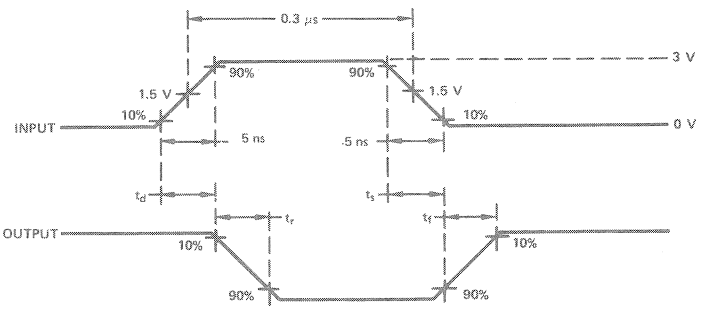
Fig. 13. SWITCHING TIMES, EACH TRANSISTOR
(75450, 75450B, 75460 ONLY)



NOTES:

A. The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{out} \approx 50\ \Omega$.

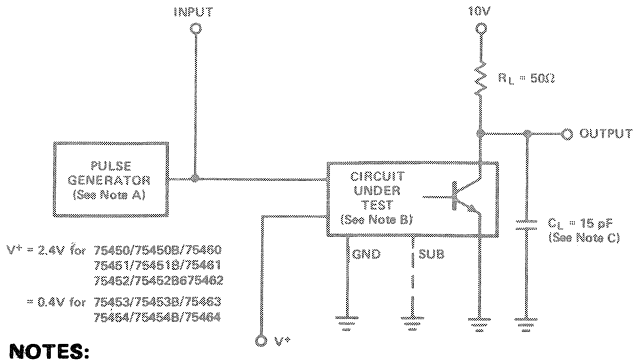
B. C_L includes probe and jig capacitance.

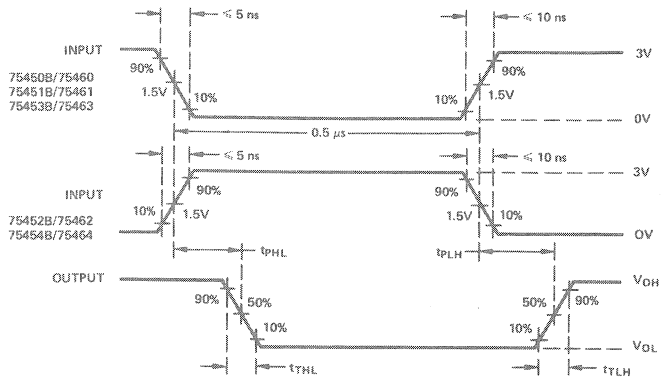


VOLTAGE WAVEFORMS

Test Circuits (Cont'd.)

Fig. 14. SWITCHING TIMES OF COMPLETE DRIVERS





VOLTAGE WAVEFORMS

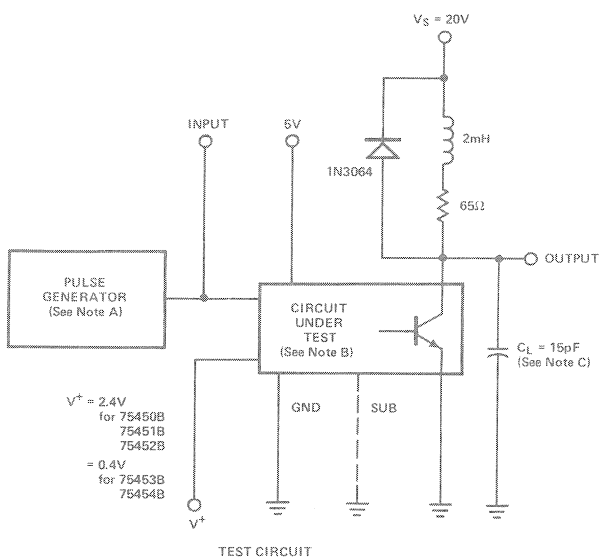
NOTES:

A. The pulse generator has the following characteristics: PRR – 1 MHz, $Z_{out} \approx 50\Omega$.

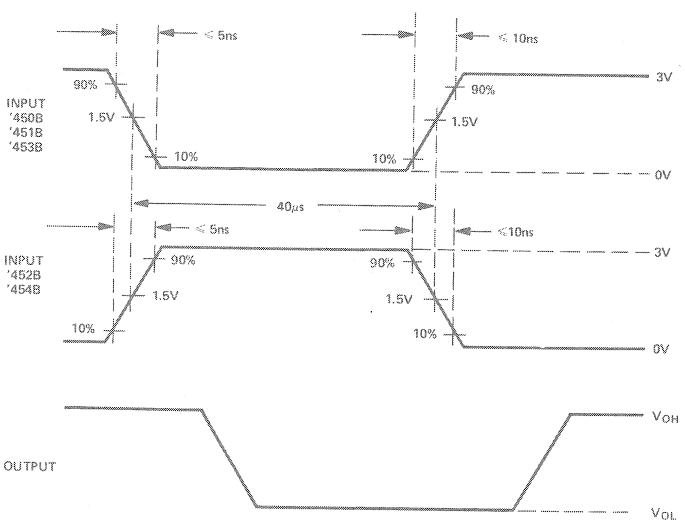
B. When testing 75450, 75450B, and 75460, connect output Y to transistor base and ground the substrate terminal.

C. C_L includes probe and jig capacitance.

Fig. 15. LATCH-UP TEST OF COMPLETE DRIVERS



TEST CIRCUIT



NOTES:

A. The pulse generator has the following characteristics: PRR = 12.5kHz, Z_{out} = 50Ω.

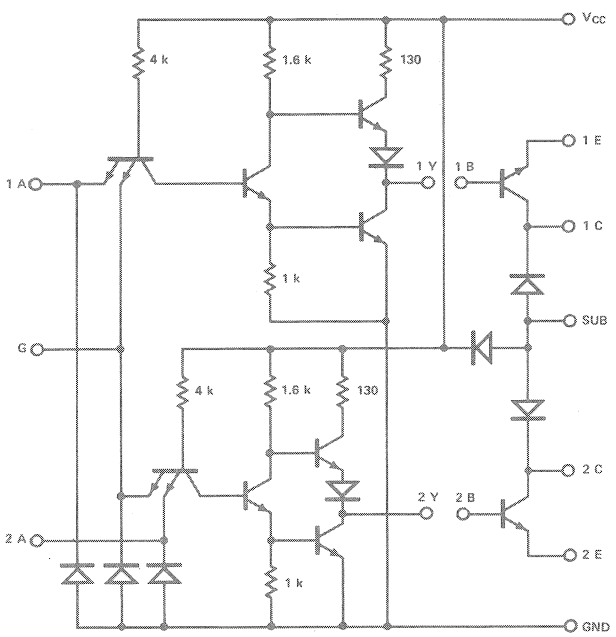
B. When testing 75450B, connect output Y to transistor base with a 500Ω resistor from there to ground, and ground the substrate terminal.

C. C_L includes probe and jig capacitance.

75450/75450B/75460

Dual Positive AND

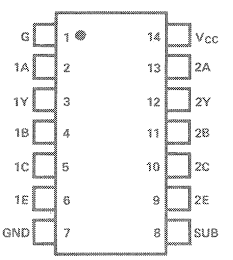
Equivalent Circuit Diagram



All resistor values in ohms.

Connection Diagram

J PACKAGE
14 LEAD PLASTIC DIP
(TOP VIEW)



Positive Logic: $Y = \overline{AG}$ (gate only)
$C = AG$ (gate and transistor)

Order Part Numbers:
75450J, 75450BJ,
75460J

Electrical Characteristics (V_{CC} = 5.0 V, T_A = 0°C to 70°C, unless otherwise noted.)

SYMBOL	PARAMETER		TEST FIGURE	CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	Input HIGH Voltage		1		2			V
V_{IL}	Input LOW Voltage		2				0.8	V
V_{CD}	Input Clamp Diode Voltage		3	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
V_{OH}	Output HIGH Voltage		2	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.3		V
V_{OL}	Output LOW Voltage		1	V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 16 mA		0.22	0.4	V
I_I	Input Current at Maximum Input Voltage	A G	4	V_{CC} = 5.25 V, V_I = 5.5 V			1 2	mA
I_{IH}	Input HIGH Current	A G	4	V_{CC} = 5.25 V, V_I = 2.4 V			40 80	μA
I_{IL}	Input LOW Current	A G	3	V_{CC} = 5.25 V, V_I = 0.4 V			−1,6 −3.2	mA
I_{OS}	Short-Circuit Output Current‡		5	V_{CC} = 5.25 V	−18		−55	mA
I_{CCH} 75450/B	Supply Current, Output HIGH		6	V_{CC} = 5.25 V, V_I = 0 V		2	4	mA
75460						2.8	4	mA
I_{CCL} 75450/B	Supply Current, Output LOW		6	V_{CC} = 5.25 V, V_I = 5 V		6	11	mA
75460						7	11	mA

†All typical values at V_{CC} = 5 V, T_A = 25°C. ‡Not more than one output should be shorted at a time.

Electrical Characteristics (V_{CC} = 5.0 V, T_A = 0°C to 70°C, unless otherwise noted.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{BR\ (CBO)}$ 75450/B	Collector-Base Breakdown Voltage	I_C = 100 μA, I_E = 0	35			V
75460			40			
$V_{BR\ (CER)}$ 75450/B	Collector-Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω	30			V
75460			40			
$V_{BR\ (CEO)}$ 75460	Collector-Emitter Breakdown Voltage (Note 8)	I_C = 10 mA, I_B = 0	25			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 μA, I_C = 0	5			V
		V_{CE} = 3 V, I_C = 100 mA, T_A = 25°C	25			
h_{FE}	Static Forward Current Transfer Ratio (Note 8)	V_{CE} = 3 V, I_C = 300 mA, T_A = 25°C	30			
		V_{CE} = 3 V, I_C = 100 mA, T_A = 0°C	20			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 0°C	25			
$V_{BE(sat)}$	Base-Emitter Voltage (Note 8)	I_B = 10 mA, I_C = 100 mA		0.85	1	V
		I_B = 30 mA, I_C = 300 mA		1.05	1.2	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage (Note 8)	I_B = 10 mA, I_C = 100 mA		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA		0.5	0.7	

†All typical values are at V_{CC} = 5 V, T_A = 25°C. Note 8: These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

AC CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C)

TTL Gates

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	75450 75460 MIN	75450 75460 TYP	75450 75460 MAX	75450B MIN	75450B TYP	75450B MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	12	C_L = 15 pF, R_L = 400 Ω		22			12	22	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				8			8	15	ns

Output Transistors

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	75450 75460 MIN	75450 75460 TYP	75450 75460 MAX	75450B MIN	75450B TYP	75450B MAX	UNIT
t_d	Delay Time	13	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(off)}$ = −1 V, C_L = 15 pF, R_L = 50 Ω		10			8	15	ns
t_r	Rise Time				16			12	20	ns
t_s	Storage Time				23			7	15	ns
t_f	Fall Time				14			6	15	ns

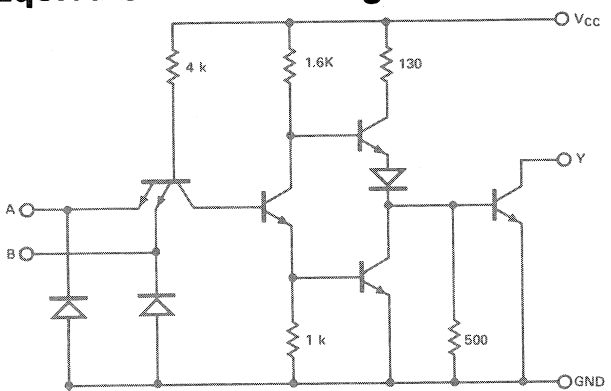
Gates and Transistors Combined

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	75450 75460 MIN	75450 75460 TYP	75450 75460 MAX	75450B MIN	75450B TYP	75450B MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	I_C = 200 mA, C_L = 15 pF, R_L = 50 Ω		40	65		20	30	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				35	50		20	30	ns
t_{TLH}	Transition Time, Output LOW to HIGH				10	20		7	12	ns
t_{THL}	Transition Time, Output HIGH to LOW				10	20		9	15	ns
V_{OH}	High-Level Output Voltage After Switching	15	V_S = 20 V, I_C ≈ 300 mA, R_{BE} = 500 Ω				V_S−6.5			mV

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

75451 / 75451B / 75461
Dual Positive AND

Equivalent Circuit Diagram



Component values shown are nominal. All resistor values in ohms.

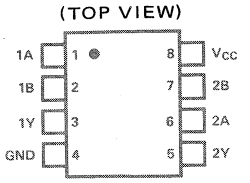
Truth Table

A	B	Y	
L	L	L	(on state)
L	H	L	(on state)
H	L	L	(on state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

Connection Diagram

P PACKAGE
8 LEAD MINIDIP
(TOP VIEW)



Positive Logic: Y = AB
Order Part Numbers:
75451P, 75451BP,
75461P

Electrical Characteristics (V_{CC} = 5.0 V, T_A = 0°C to 70°C, unless otherwise noted.)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	Input HIGH Voltage	7		2			V
V_{IL}	Input LOW Voltage	7				0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = 4.75 V, V_{IL} = 0.8 V			-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = 4.75 V, V_{OH} = 30 V, V_{IH} = 2 V			100	μA
V_{OL}	Output LOW Voltage	7	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = 5.25 V, V_I = 5.5 V			1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Input LOW Current	8	V_{CC} = 5.25 V, V_I = 0.4 V		-1.0	-1.6	mA
I_{CCH} 75451B	Supply Current, Output HIGH	10	V_{CC} = 5.25 V, V_I = 5 V		7.0	11	mA
I_{CCH} 75461					8	11	
I_{CCL} 75451B	Supply Current, Output LOW	10	V_{CC} = 5.25 V, V_I = 0 V		52	65	mA
I_{CCL} 75461					61	76	

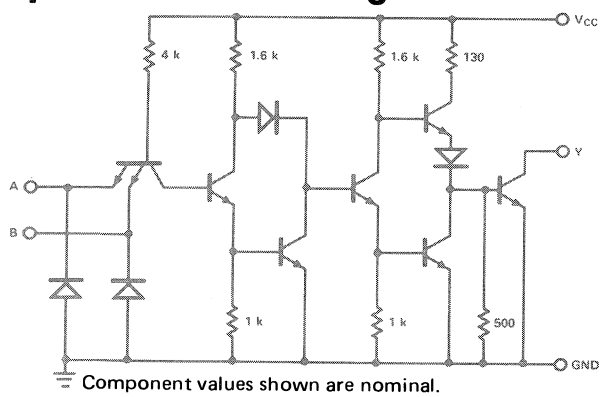
†All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	75451 75461 MIN	75451 75461 TYP	75451 75461 MAX	75451B MIN	75451B TYP	75451B MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		45	55		18	25	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				30	40		18	25	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	20		5	8	ns
t_{THL}	Transition Time, Output HIGH to LOW				10	20		7	12	ns
V_{OH}	High-Level Output Voltage After Switching	15	V_S = 20 V, $I_C \approx$ 300 mA				V_S–6.5			mV

75452/75452B/75462
Dual Positive NAND

Equivalent Circuit Diagram



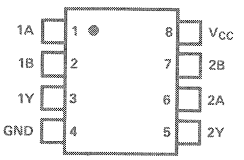
Component values shown are nominal.

Truth Table

A	B	Y	
L	L	H	(off state)
L	H	H	(off state)
H	L	H	(off state)
H	H	L	(on state)

Connection Diagram

P PACKAGE
8 LEAD MINIDIP
(TOP VIEW)



Positive Logic: $Y = \overline{AB}$
Order Part Numbers:
75452P, 75452BP,
75462P

Electrical Characteristics (V_{CC} = 5.0V, T_A = 0°C to 70°C, unless otherwise noted.)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	Input HIGH Voltage	7		2			V
V_{IL}	Input LOW Voltage	7				0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = 4.75V, I_I = −12 mA			−1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = 4.75V, V_{OH} = 30V, V_{IL} = 0.8V			100	μA
V_{OL}	Output LOW Voltage	7	V_{CC} = 4.75V, V_{IH} = 2V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = 4.75V, V_{IH} = 2V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = 5.25V, V_I = 5.5V			1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = 5.25V, V_I = 2.4V			40	μA
I_{IL}	Input LOW Current	8	V_{CC} = 5.25V, V_I = 0.4V		−1.0	−1.6	mA
I_{CCH} 75452/B	Supply Current, Output HIGH	10	V_{CC} = 5.25V, V_I = 0V		11	14	mA
I_{CCH} 75462					13	17	
I_{CCL} 75452/B	Supply Current, Output LOW	10	V_{CC} = 5.25V, V_I = 5V		56	71	mA
I_{CCL} 75462					65	76	

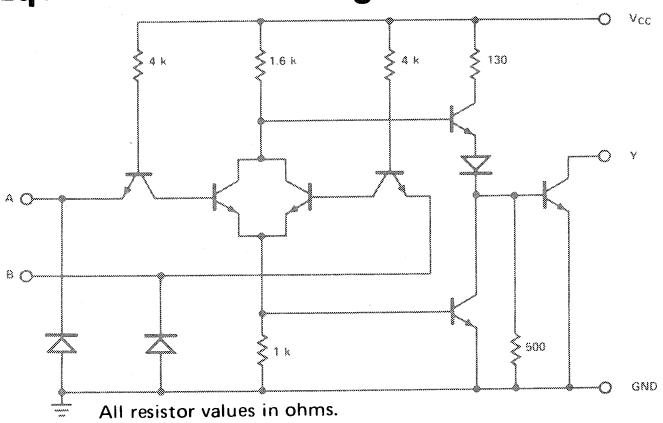
†All typical values are at V_{CC} = 5V, T_A = 25°C.

AC CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	75452 75462 MIN	75452 75462 TYP	75452 75462 MAX	75452B MIN	75452B TYP	75452B MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		50	65		26	35	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				40	50		24	35	ns
t_{TLH}	Transition Time, Output LOW to HIGH				12	25		5	8	ns
t_{THL}	Transition Time, Output HIGH to LOW				15	20		7	12	ns
V_{OH}	High-Level Output Voltage After Switching	15	V_S = 20 V, $I_C \approx$ 300 mA				V_S−6.5			mV

75453/75453B/75463
Dual Positive OR

Equivalent Circuit Diagram



All resistor values in ohms.

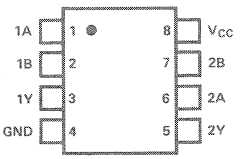
Truth Table

A	B	Y	
L	L	L	(on state)
L	H	H	(off state)
H	L	H	(off state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

Connection Diagram

P PACKAGE
8 LEAD MINIDIP
(TOP VIEW)



Positive Logic: Y = A + B

Order Part Numbers:
75453P, 75453BP,
75463P

Electrical Characteristics (V_{CC} = 5.0V, T_A = 0°C to 70°C, unless otherwise noted)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	Input HIGH Voltage	7		2			V
V_{IL}	Input LOW Voltage	7				0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = 4.75V, I_I = −12 mA			−1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = 4.75V, V_{OH} = 30V, V_{IH} = 2V			100	μA
V_{OL}	Output LOW Voltage	7	V_{CC} = 4.75V, V_{IL} = 0.8V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = 4.75V, V_{IL} = 0.8V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = 5.25V, V_I = 5.5V			1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = 5.25V, V_I = 2.4V			40	μA
I_{IL}	Input LOW Current	8	V_{CC} = 5.25V, V_I = 0.4V		−1.0	−1.6	mA
I_{CCH}	Supply Current, Output HIGH	11	V_{CC} = 5.25V, V_I = 5V		8.0	11	mA
I_{CCL} 75453/B	Supply Current, Output LOW	11	V_{CC} = 5.25V, V_I = 0V		54	68	mA
I_{CCL} 75463	Supply Current, Output LOW	11	V_{CC} = 5.25V, V_I = 0V		63	76	mA

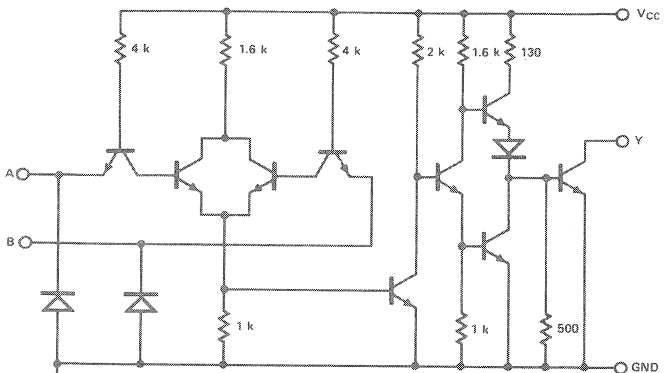
† All typical values are at V_{CC} = 5V, T_A = 25°C.

AC CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	75453 75463 MIN	75453 75463 TYP	75453 75463 MAX	75453B MIN	75453B TYP	75453B MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		45	55		18	25	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		30	40		16	25	ns
t_{TLH}	Transition Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		8	25		5	8	ns
t_{THL}	Transition Time, Output HIGH to LOW	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		10	25		7	12	ns
V_{OH}	High-Level Output Voltage After Switching	15	V_S = 20 V, $I_C \approx$ 300 mA				V_S−6.5			mV

75454/75454B/75464
Dual Positive NOR

Equivalent Circuit Diagram



Component values shown are nominal. All resistor values in ohms.

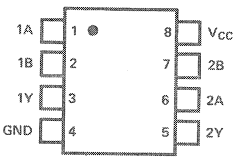
Truth Table

A	B	Y	
L	L	H	(off state)
L	H	L	(on state)
H	L	L	(on state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level

Connection Diagram

P PACKAGE
8 LEAD MINIDIP
(TOP VIEW)



Positive Logic: $Y = \overline{A + B}$
Order Part Numbers:
75454P, 75454BP,
75464P

Electrical Characteristics (V_{CC} = 5.0V ±5%, T_A = 0°C to 70°C, unless otherwise noted)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	Input HIGH Voltage	7		2			V
V_{IL}	Input LOW Voltage	7				0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = 4.75V, I_I = −12 mA			−1.5	V
I_{OH}	Output HIGH Voltage	7	V_{CC} = 4.75V, V_{OH} = 30V, V_{IL} = 0.8V			100	μA
V_{OL}	Output LOW Voltage	7	V_{CC} = 4.75V, V_{IH} = 2V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = 4.75V, V_{IH} = 2V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = 5.25V, V_I = 5.5V			1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = 5.25V, V_I = 2.4V			40	μA
I_{IL}	Input LOW Current	8	V_{CC} = 5.25V, V_I = 0.4V		−1.0	−1.6	mA
I_{CCH}	75454/B	Supply Current, Output HIGH	11	V_{CC} = 5.25V, V_I = 0V		13	17	mA
	75464					14	19	
I_{CCL}	75454/B	Supply Current Output LOW	11	V_{CC} = 5.25V, V_I = 5V		61	79	mA
	75464					72	85	

†All typical values are at V_{CC} = 5V, T_A = 25°C.

AC CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	75454 75464 MIN	75454 75464 TYP	75454 75464 MAX	75454B MIN	75454B TYP	75454B MAX	UNIT
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		50	65		27	35	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				40	50		24	35	ns
t_{TLH}	Transition Time, Output LOW to HIGH				12	20		5	8	ns
t_{THL}	Transition Time, Output HIGH to LOW				15	20		7	12	ns
V_{OH}	High-Level Output Voltage After Switching	15	V_S = 20 V, $I_C \approx$ 300 mA				V_S−6.5			mV

Section V
Timers

D555
Dual Timer

Features

- REPLACES TWO 555 TIMERS
- TIMING FROM MICROSECONDS TO HOURS
- OUTPUT COMPATIBLE WITH TTL, CMOS, HiNIL LOGIC
- HIGH OUTPUT CURRENT DRIVE CAPABILITY
- EXCELLENT MATCHING BETWEEN TIMERS

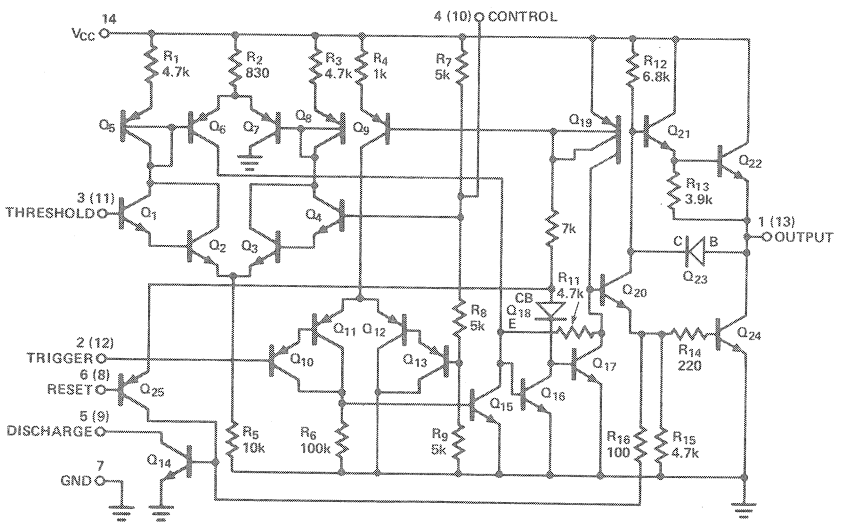
Description

The Teledyne D555 Dual Timer consists of two independent 555 type timers on a single monolithic chip. Each timing section is capable of functioning as an accurate time delay or astable oscillator. Independent trigger, reset, and timing terminals are provided for each section. The related time interval is precisely set by an external R-C combination.

Separate outputs are capable of driving various logic families, including TTL, CMOS, and HiNIL, with up to 200mA of source or sink current. Trigger and Reset inputs are logic-level compatible.

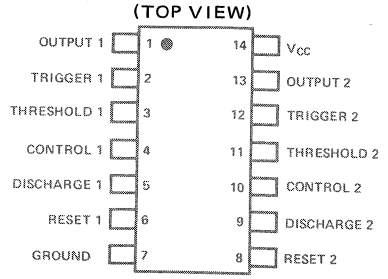
The D555 is primarily intended for industrial control applications including pulse generation, pulse shaping, time delay, clock generation, and various pulse modulation schemes. The D555 Dual Timer is intended for operation over a temperature range of 0°C to +70°C.

Equivalent Circuit Diagram



Connection Diagram

J PACKAGE
14 LEAD PLASTIC DIP
(TOP VIEW)



Order Part Number:
D555CJ

Absolute Maximum Ratings

Supply Voltage	18V
Power Dissipation (Note 1)	530mW
Storage Temperature Range	−65°C/+150°C
Operating Temperature Range	0°C/+70°C
Lead Soldering Temperature (60 sec)	300°C
Junction Temperature	150°C

NOTES:

1. Rating is for the total package at an ambient temperature of up to 70°C.
2. Supply current when output is high is typically 1.0mA less.
3. Tested at V_{CC} = 5V and V_{CC} = 15V.
4. This will determine the maximum value of $R_A + R_B$. For 15V operation, the maximum total R = 20MΩ.
5. Matching characteristics refer to the difference between performance characteristics of each timer section.

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage		4.5		16	V
Supply Current (Each Timer Section)	Low State Output, Note 2 V_{CC} = 5V, R_L = ∞ V_{CC} = 15V, R_L = ∞		 3 10	 6 15	 mA mA
Total Supply Current (Both Timer Sections)	Low State Output V_{CC} = 5V, R_L = ∞ V_{CC} = 15V, R_L = ∞		 6 20	 12 30	 mA mA
Timing Error Initial Accuracy Drift with Temperature Drift with Supply Voltage	R_A, R_B = 1kΩ to 100kΩ, C = 0.1μF, Note 3		 1.0 50 0.1		 % ppm/°C %/V
Threshold Voltage			2/3		x V_{CC}
Trigger Voltage	V_{CC} = 5V V_{CC} = 15V		1.67 5.0		V V
Trigger Current			0.5		μA
Reset Voltage		0.4	0.7	1.0	V
Reset Current			0.1		mA
Threshold Current	Note 4		30	100	nA
Control Voltage Level	V_{CC} = 5V V_{CC} = 15V	2.60 9.0	3.33 10.0	4.0 11.0	V V
Output Voltage (Low)	V_{CC} = 5V I_{sink} = 5.0mA V_{CC} = 15V I_{sink} = 10mA I_{sink} = 50mA I_{sink} = 100mA I_{sink} = 200mA		 0.25 0.1 0.4 2.0 2.5	 0.35 0.25 0.75 2.5	 V V V V V
Output Voltage (High)	I_{source} = 100mA V_{CC} = 5V V_{CC} = 15V I_{source} = 200mA V_{CC} = 15V	 2.75 12.75	 3.3 13.3 12.5		 V V V
Rise Time of Output Fall Time of Output Discharge Leakage Current			100 100 20	 100	ns ns nA
Matching Characteristics Initial Timing Accuracy Timing Drift with Temperature	Note 5		 0.2 ±10		 % ppm/°C

NOTES:

1. Rating is for the total package at an ambient temperature of up to 70°C.
2. Supply current when output is high is typically 1.0mA less.
3. Tested at V_{CC} = 5V and V_{CC} = 15V.
4. This will determine the maximum value of $R_A + R_B$. For 15V operation, the maximum total R = 20MΩ.
5. Matching characteristics refer to the difference between performance characteristics of each timer section.

Typical Performance Characteristics (Each Timer Section)

MINIMUM TRIGGER PULSE WIDTH

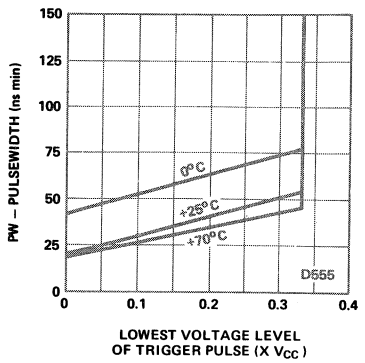


Figure 1

SUPPLY CURRENT (BOTH TIMER SECTIONS)

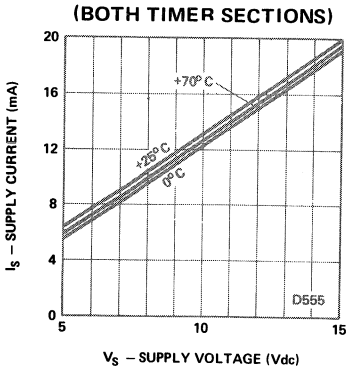


Figure 2

HIGH OUTPUT VOLTAGE

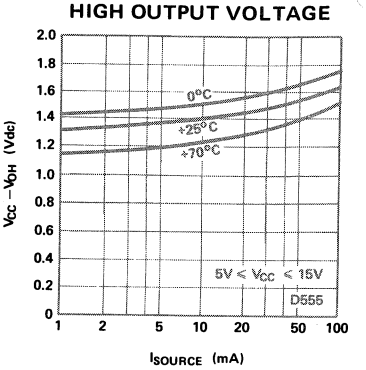


Figure 3

LOW OUTPUT VOLTAGE

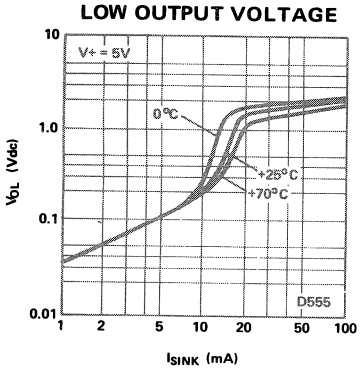


Figure 4

LOW OUTPUT VOLTAGE

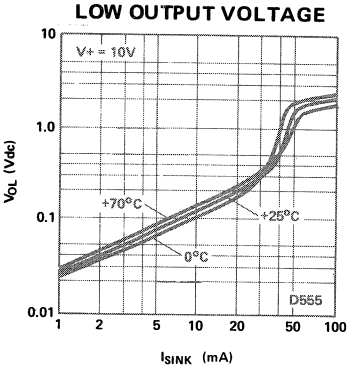


Figure 5

LOW OUTPUT VOLTAGE

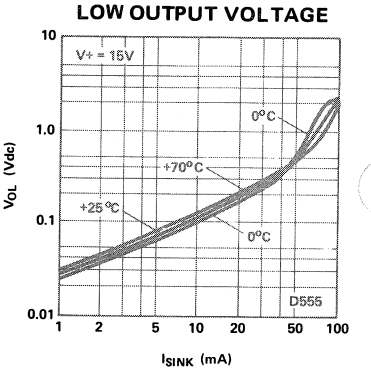


Figure 6

DELAY TIME VS. SUPPLY VOLTAGE

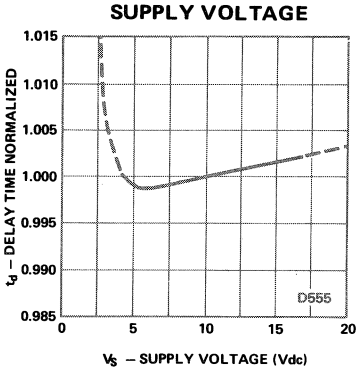


Figure 7

DELAY TIME VS. TEMPERATURE

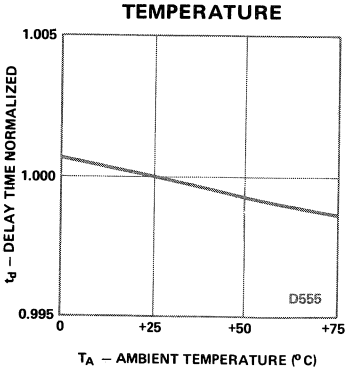


Figure 8

PROPAGATION DELAY VS. TRIGGER VOLTAGE

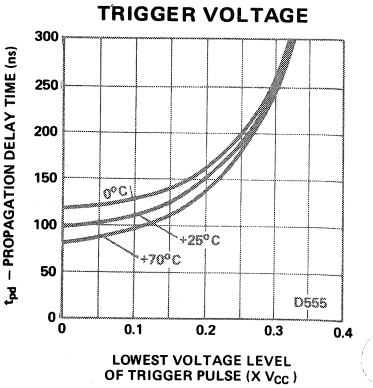


Figure 9

Typical Applications

DESCRIPTION OF CIRCUIT CONTROLS

Output

The output logic level is normally in a "low" state, and goes "high" during the timing cycle.

Trigger

The timing cycle is initiated by lowering the dc level at the trigger terminal below 1/3 V_{CC}. Once triggered, the circuit is immune to additional triggering until the timing cycle is completed.

Threshold

The timing cycle is completed when the voltage level at the threshold terminal reaches 2/3 V_{CC}. At this point, the threshold comparator changes state, resets the internal flip-flop, and initiates the discharge cycle.

Control or FM

The timing cycle or the frequency of oscillation can be controlled or modulated by applying a dc control voltage to pin 4 or 10. This terminal is internally biased at 2/3 V_{CC}. The control signal for frequency modulation or pulse-width modulation is applied to this terminal. When not in use, the control terminals should be ac grounded through 0.01μF decoupling capacitors.

Discharge

This terminal corresponds to the collector of the discharge transistor. During the charging cycle, this terminal behaves as an open-circuit; during discharge, it becomes a low impedance path to ground.

Reset

The timing cycle can be interrupted by grounding the reset terminal. When the reset signal is applied, the output goes "low" and remains in that state while the reset voltage is applied. When the reset signal is removed, the output remains "low" until re-triggered. When not used, the reset terminals should be connected to V_{CC} in order to avoid any possibility of false resetting. When the timing circuits are operated in the astable mode, the reset terminals can be used for "on" and "off" keying of the oscillations.

SPECIAL APPLICATIONS CONSIDERATIONS

Triggering

The device triggers on the negative going edge of a low going pulse. The trigger pulse must be of shorter duration than the "RC" time interval. If the trigger is held low, the output will stay high until trigger is driven high again.

Timing Drift with Temperature

The timer in the monostable mode has a timing drift of 50 PPM/°C typical. In the astable mode, since both comparators of the device are used, the drift is somewhat greater. (Typically 150 PPM/°C drift)

Maximum Oscillation Frequency

The D555 timer is capable of oscillating at up to 300kHz. However, for temperature stability the limit should be around 200kHz.

Duty Cycle

When expressed as a ratio of output "true" time to total cycle time, the duty cycle is normally greater than 50%. However, by adding a diode as shown, a duty cycle of less than 50% can be achieved.

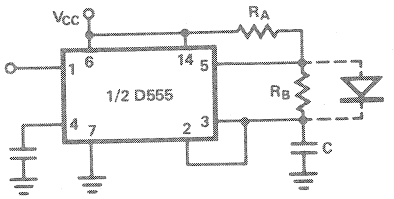


Figure 1

Latch Up When Driving an Inductive Load

A negative voltage at pin 1 can cause a latch up. The solution is to add two diodes as shown. This circuit prohibits a negative voltage from reaching pin 1.

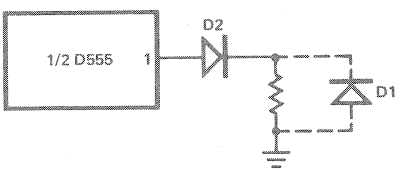


Figure 2

Monostable Operation

In this mode of operation, the timer functions as a one-shot. Referring to Figure 3 the external capacitor is initially held discharged by a transistor inside the timer.

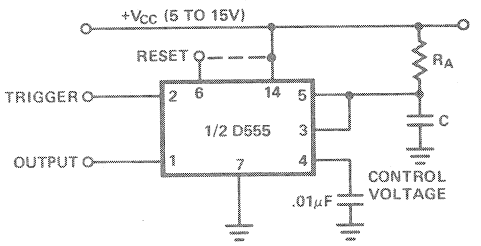


Figure 3

Upon application of a negative trigger pulse to pin 2, the flip-flop is set which releases the short circuit across the external capacitor and drives the output high. The voltage across the capacitor, now, increases exponentially with the time constant $\tau = R_A C$. When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which in turn discharges the capacitor rapidly and drives the output to its low state. Figure 4 shows the actual waveforms generated in this mode of operation.

The circuit triggers on a negative going input signal when the level reaches 1/3 V_{CC}. Once triggered, the circuit will remain in this state until the set time is elapsed, even if it is triggered again during this interval. The time that the output is in the high state is given by $t = 1.1\ R_A C$. Notice that since the charge rate, and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is inde-

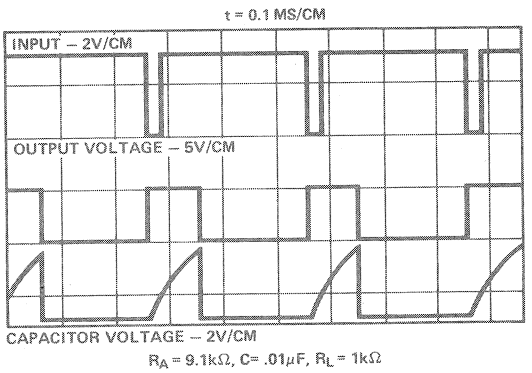


Figure 4

Typical Applications (Cont'd.)

pendent of supply. Applying a negative pulse simultaneously to the reset terminal (pin 6) and the trigger terminal (pin 2) during the timing cycle discharges the external capacitor. The timing cycle will now commence on the positive edge of the reset pulse.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false resetting.

Astable Operation

If the circuit is connected as shown in Figure 5 (pins 3 and 2 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

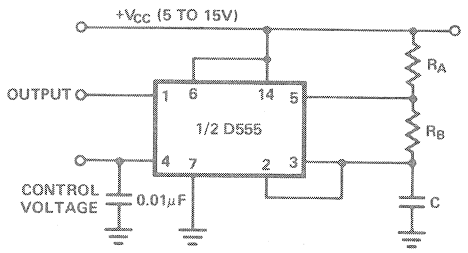


Figure 5

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 6 shows waveforms generated in this mode of operation.

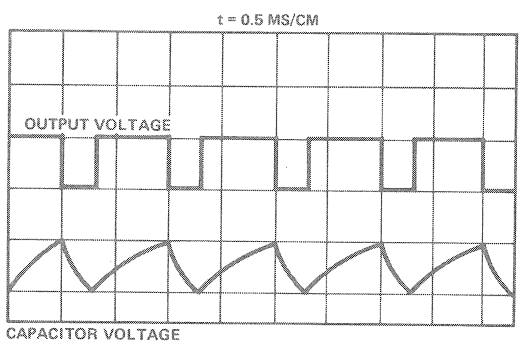


Figure 6

The charge time (output high) is:

$$t_1 = 0.693\ (R_A + R_B)C$$

The discharge time (output low) is:

$$t_2 = 0.693\ (R_B)C$$

The total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C}$$

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

Missing Pulse Detector

Using the circuit of Figure 7, the timing cycle is continuously reset by the input pulse train. A change in frequency, or a missing pulse, allows completion of the timing cycle which causes a change in the output level. For this application, the time delay should be set to be slightly longer than the normal time between pulses. Figure 8 shows the waveforms seen in this mode of operation.

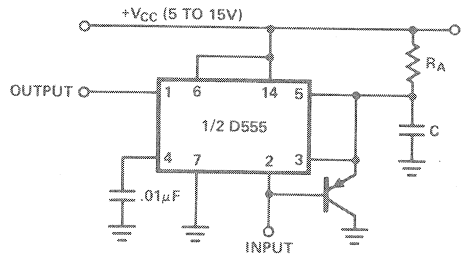


Figure 7

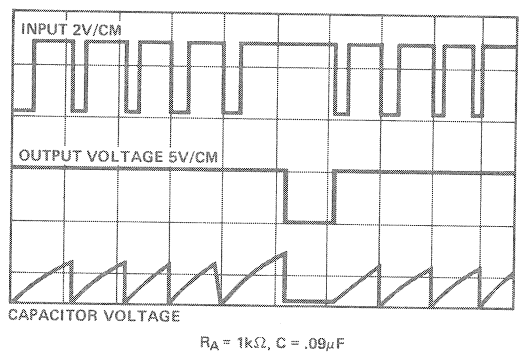


Figure 8

Long Time Delays

In the D555 timer the timing is a function of the charging rate of the external capacitor. For long time delays expensive capacitors with extremely low leakage are required. The practicality of the components involved limits the time between pulses to something in the neighborhood of ten minutes.

To achieve longer time periods both halves may be connected in tandem with a "Divide-by" network in between. The first timer section operates in an oscillatory mode with a period of $1/f_0$.

This signal is then applied to a "Divide-by-N" network to give an output with the period of N/f_0. This can then be used to trigger the second half of the D555. The total time delay is now a function of N and f_0.

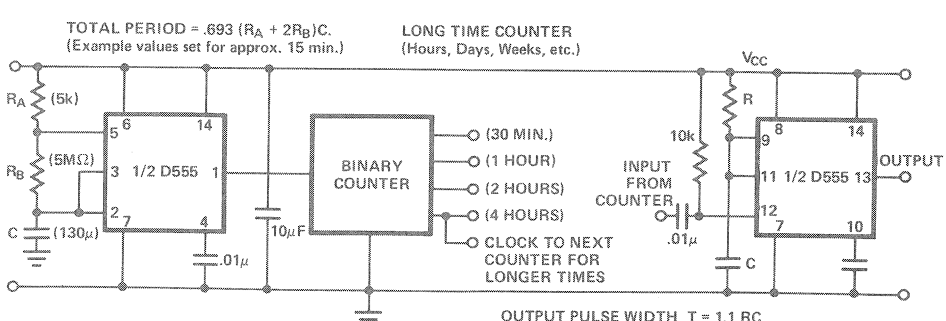


Figure 9

Typical Applications (Cont'd.)

Keyed Oscillator

One of the timer sections of the D555 can be operated in its free-running mode, and the other timer section can be used to key it "on" and "off". A recommended circuit connection is shown in Figure 10.

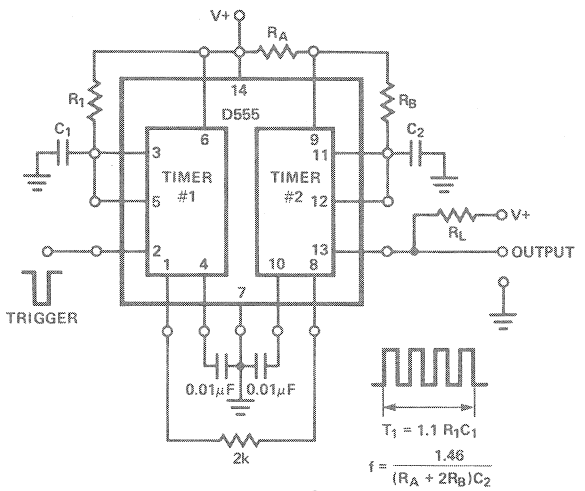


Figure 10

Frequency Divider and Pulse Shaper

If the frequency of the input is known, each timer section of the D555 can be used as a frequency divider by adjusting the length of its timing cycle. If the timing interval T_1 (= 1.1 R_1 C_1) is larger than the period of the input pulse trigger, then only those input pulses which are spaced more than 1.1 R_1 C_1 will actually trigger the circuit.

If desired, the remaining timer section can be used as a "pulse-shaper" to adjust the duty cycle of the output waveform. As seen in Figure 11, Timer 1 is used as the frequency divider section and Timer 2 is used as the pulse-shaper. Corresponding waveforms are shown in Figure 12.

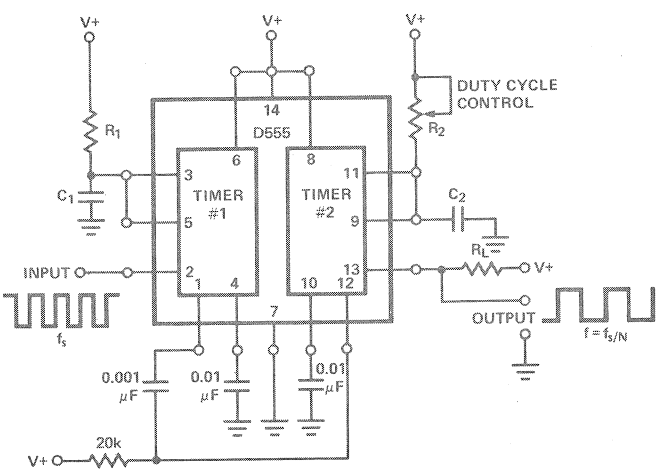


Figure 11

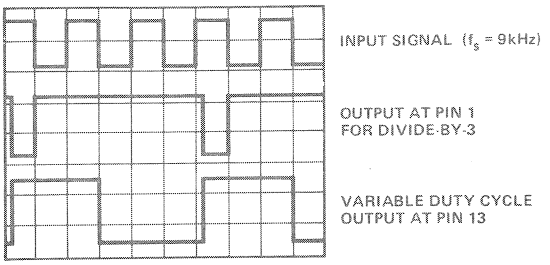


Figure 12

Pulse Position Modulation

When a timer section of the D555 is operated in its astable mode, the period of the output pulse train can be varied by applying a modulation voltage to the corresponding modulation control terminal. In this manner, the repetition rate of the output pulse train can be varied. This output can be used to drive a second timer section operating in the monostable mode, resulting in a pulse-position modulated output. Typical transfer characteristics between the timing cycle and the modulation voltage are given in Figure 13.

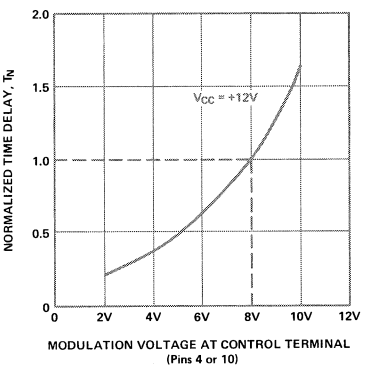


Figure 13

Pulse Width Modulation (PWM)

In this application, the timer is connected in the monostable mode as shown in Figure 14. This circuit is triggered with a continuous pulse train and the threshold voltage is modulated by the signal applied to the control voltage terminal (pin 4). This has the effect of modulating the pulse width as the control voltage varies.

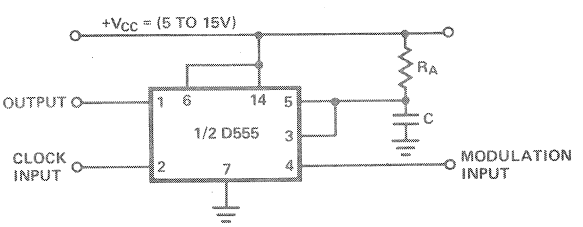


Figure 14

556
Dual Timer

Features

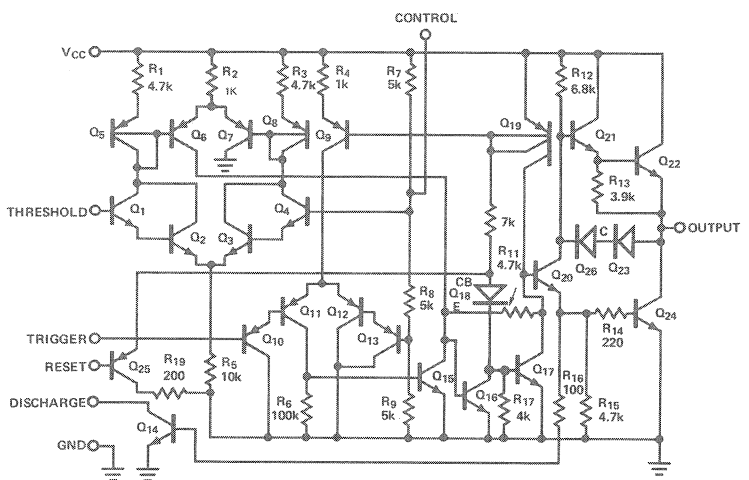
- TIMING FROM MICROSECONDS THROUGH HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- ADJUSTABLE DUTY CYCLE
- OUTPUT DRIVES TTL
- HIGH CURRENT OUTPUT CAN SOURCE OR SINK 150mA
- TEMPERATURE STABILITY OF 0.005%/°C

Description

The Teledyne 556 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode, delay time is precisely controlled by only two external parts: a resistor and a capacitor. For operation as an oscillator, both the free running frequency and the duty cycle are accurately controlled by two external resistors and a capacitor.

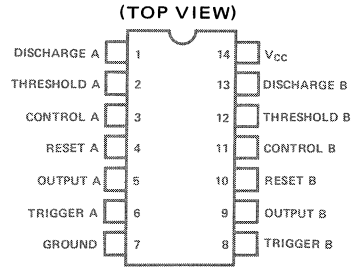
Terminals are provided for triggering and resetting. The circuit will trigger and reset on falling waveforms. The output can source or sink up to 150mA or drive TTL circuits. The 556 circuit is intended for operation over the temperature range of 0°C to +70°C.

Equivalent Circuit Diagram



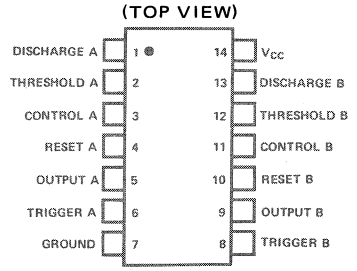
Connection Diagrams

L PACKAGE
14 LEAD CERDIP
(TOP VIEW)



Order Part Number:
556CL

J PACKAGE
14 LEAD PLASTIC DIP
(TOP VIEW)



Order Part Number:
556CJ

Absolute Maximum Ratings

Supply Voltage	+18V
Power Dissipation (Note 1)	530mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

NOTE:

1. Rating is for the total package at ambient temperature up to 70° C.

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		4.5		16	V
Supply Current (Each Side)	V_{CC} = 5V, R_L = ∞ V_{CC} = 15V, R_L = ∞ Low State (1)		3 10	6 14	mA mA
Timing Error (Free Running) Initial Accuracy Drift with Temperature Drift with Supply Voltage	R_A, R_B = 2 kΩ to 100 kΩ C = 0.1 μF (2)		 2.25 150 0.3		 % ppm/°C %/Volt
Timing Error (Monostable) Initial Accuracy Drift with Temperature Drift with Supply Voltage	R_A, R_B = 2 kΩ to 100 kΩ C = 0.1 μF (2)		 0.75 50 0.1		 % ppm/°C %/Volt
Threshold Voltage			2/3		X V_{CC}
Trigger Voltage	V_{CC} = 15V V_{CC} = 5V		5 1.67		V V
Trigger Current			0.5		μA
Reset Voltage		0.4	0.7	1.0	V
Reset Current			0.1		mA
Threshold Current	(3)		0.03	0.1	μA
Control Voltage Level	V_{CC} = 15V V_{CC} = 5V	9.0 2.6	10 3.33	11 4	V V
Output Voltage (low) I_{SINK} = 10 mA I_{SINK} = 50 mA I_{SINK} = 100 mA I_{SINK} = 150 mA V_{CC} = 5V I_{SINK} = 5 mA	V_{CC} = 15V		 0.1 0.4 2 2.5 0.25	 0.25 0.75 2.75 0.35	 V V V V
Output Voltage (high) I_{SOURCE} = 150 mA V_{CC} = 15V I_{SOURCE} = 100 mA V_{CC} = 15V V_{CC} = 5V		 12.75 2.75	 12.5 13.3 3.3		 V V V
Rise Time of Output			100		ns
Fall Time of Output			100		ns
Discharge Leakage Current			.02	.1	μA

Electrical Characteristics (Cont'd.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Matching Characteristics Between Each Section					
Initial Timing Accuracy			0.1	0.2	%
Timing Drift with Temperature			±10		ppm/°C
Drift with Supply Voltage			0.2	0.5	%/Volt

NOTES: 1. Supply current when output high typically 1mA less (each side). 2. Tested at V_{CC} = 5V and V_{CC} = 15V. 3. This will determine the maximum value of $R_A + R_B$. For 15V operation, the maximum total R = 20MΩ.

Typical Performance Characteristics

MINIMUM TRIGGER PULSE WIDTH

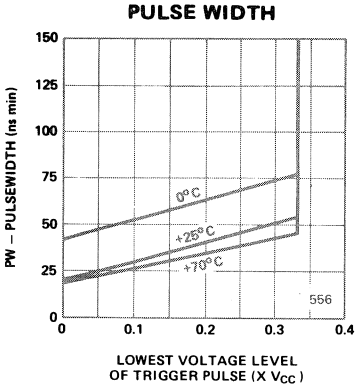


Figure 1

SUPPLY CURRENT (BOTH TIMER SECTIONS)

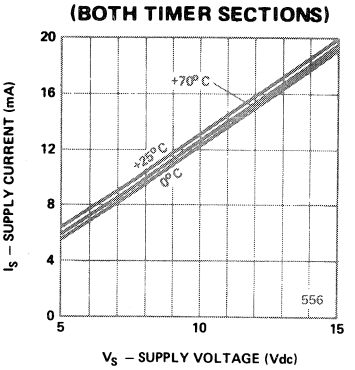


Figure 2

HIGH OUTPUT VOLTAGE

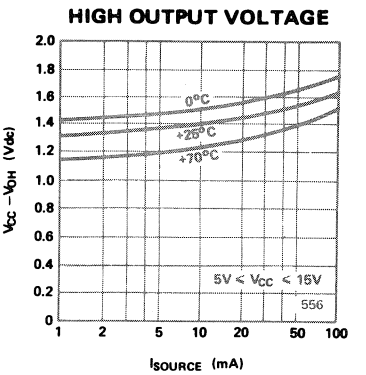


Figure 3

LOW OUTPUT VOLTAGE

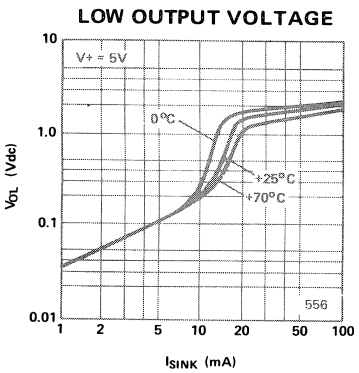


Figure 4

LOW OUTPUT VOLTAGE

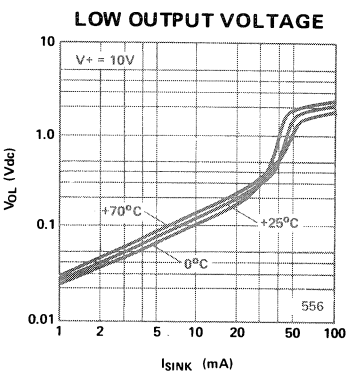


Figure 5

LOW OUTPUT VOLTAGE

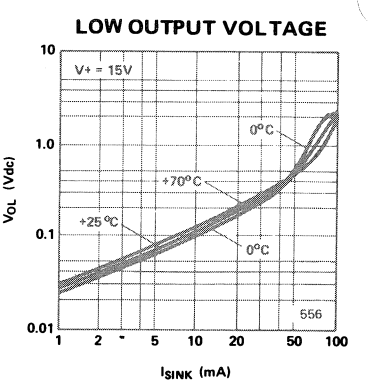


Figure 6

DELAY TIME VS. SUPPLY VOLTAGE

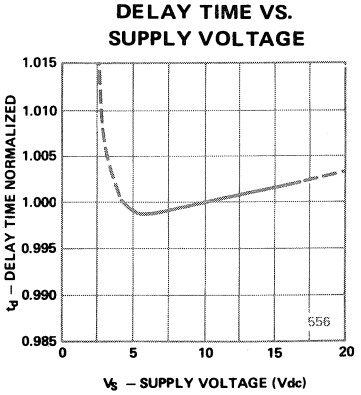


Figure 7

DELAY TIME VS. TEMPERATURE

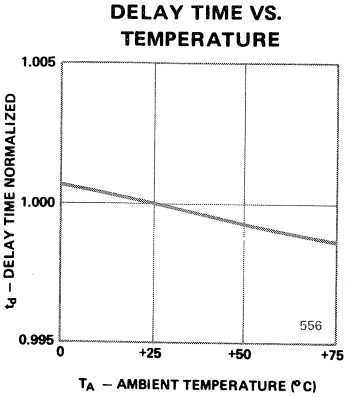


Figure 8

PROPAGATION DELAY VS. TRIGGER VOLTAGE

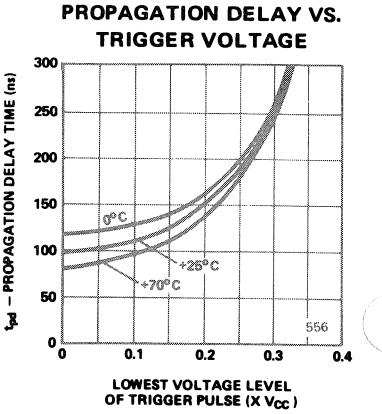
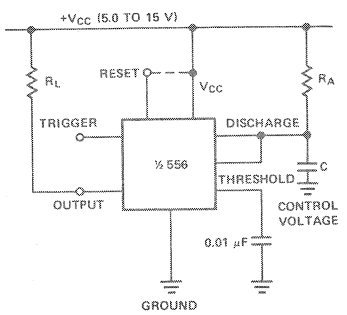


Figure 9

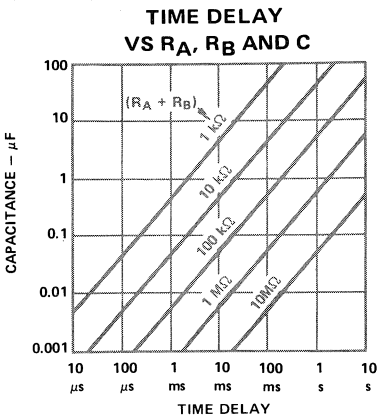
Typical Applications

MONOSTABLE OPERATION

In this mode, the timer functions as one-shot. The external capacitor is initially held discharged by a transistor internal to the timer. Applying a negative trigger pulse to Pin 2 sets the flip-flop, driving the output high and releasing the short-circuit across the external capacitor. The voltage across the capacitor increases with time constant r = $R_A C$ to 2/3 V_{CC}, where the comparator resets the flip-flop and discharges the external capacitor. The output is now in the low state.

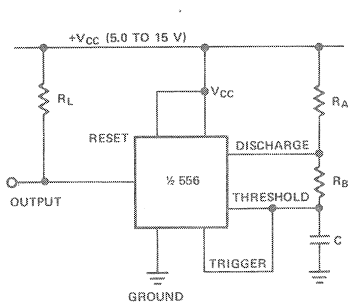


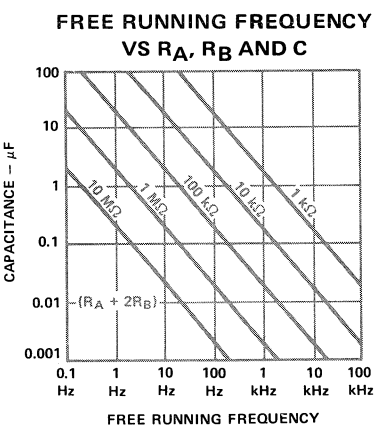
Circuit triggering takes place when the negative-going trigger pulse reaches 1/3 V_{CC} and the circuit stays in the output high state until the set time elapses. The time the output remains in the high state is 1.1 $R_A C$ and can be determined by the graph. A negative pulse applied to Pin 4 (reset) during the timing cycle will discharge the external capacitor and start the cycle over again beginning on the positive-going edge of the reset pulse. If reset function is not used, Pin 4 should be connected to V_{CC} to avoid false resetting.



FREE RUNNING OPERATION (Astable)

With the circuit connected as shown and it will trigger itself and free run as a multivibrator. The external capacitor charges thru R_A and R_B and discharges thru R_B only. Thus the duty cycle is set by the ratio of these two resistors, and the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. Charge and discharge times, and therefore frequency, are independent of supply voltage. The free running frequency versus R_A, R_B, and C is shown in the graph.





Section VI

Glossary of Terms
Package Information
Product Index

Glossary of Terms

Average Input Offset Current t° Coefficient—(Op Amps) Change in input offset current divided by change in ambient temperature producing it.

Bandwidth—(Op Amps) Frequency at which voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

Common Mode Firing Voltage—(Comparators) CM input voltage that exceeds dynamic range of inputs with strobe enabled resulting in output switching states.

Common Mode Input Resistance—(Op Amps) Resistance looking into both inputs tied together.

Common Mode Recovery Time—(Comparators) Time from turn off of CM signal to analog input threshold of earliest sense line pulse signal that can be processed normally. Processed normally refers to bi-polar signals greater than or less than input threshold with corresponding proper output.

Common Mode Rejection Ratio CMRR—(Op Amps) Ratio of change of input offset voltage to input common mode voltage change producing it.

Current-Limit Sense Voltage—(Regulators) Voltage across current limit terminals required to cause regulator to current-limit with short-circuited output. This voltage is used to determine value of external current-limit resistor when external booster transistors are used.

Differential Input Offset Current—(Comparators) Absolute difference in two input bias currents of one differential input.

Differential Input Overload Recovery Time—(Comparators) Time necessary for device to recover from 2V differential pulse ($t_f = t_r =$ 20ns) prior to strobe enable signal.

Differential Input Threshold Voltage—(Comparators) DC input voltage which forces logic output to logic threshold voltage (~1.5V) level.

Dropout Voltage—(Regulators) Input-output voltage differential at which circuit ceases to regulate against further reductions in input voltage.

Equivalent Input Common Mode Noise Voltage—(Comparators) Change in input offset voltage due to common mode input noise.

Full Power Bandwidth—(Op Amps) Maximum frequency at which full sinewave output might be obtained.

Harmonic Distortion—(Op Amps) Percentage of harmonic distortion being defined as 100 times ratio of RMS sum of harmonics to fundamental.

% harmonic distortion =

$$\frac{(V_2^2 + V_3^3 + V_4^2 + \ldots)^{1/2}\ (100\%)}{V_1}$$

where V_1 is RMS amplitude of fundamental and V_2, V_3, V_4, . . . are RMS amplitudes of individual harmonics.

Input Bias Current—(Comparators) DC current which flows into each input pin with differential input of 0V. —(Op Amps) Average of the two input currents at zero input voltage.

Input Capacitance—(Op Amps) Capacitance looking into either input terminal with other grounded.

Input Current—(Op Amps) Current into an input terminal.

Input Impedance—(Op Amps) Ratio of input voltage to input current under stated conditions for source resistance (R_S) and load resistance (R_L).

Input Noise Voltage—(Op Amps) Square root of mean square narrow-band noise voltage referred to input.

Input Offset Current—(Comparators) Absolute value of difference between two input currents for which output will be driven higher or lower than specified voltages. —(Op Amps) Difference in currents into two input terminals with output at zero volts.

Input Offset Voltage—(Comparators) Absolute value of voltage between input terminals required to make output voltage greater or less than specified voltages. —(Op Amps) Voltage which must be applied between input terminals to obtain zero output voltage. Input offset voltage may also be defined for case where two equal resistances are inserted in series with input leads.

Input-Output Voltage Differential—(Regulators) Range of voltage difference between supply voltage and regulated output voltage over which regulator will operate.

Input Resistance—(Op Amps) Resistance looking into either input terminal with other grounded.

Input Voltage Range—(Comparators) Range of voltage on input terminals (common mode) over which offset specifications apply. —(Op Amps) Range of voltages on input terminals for which amplifier operates within specifications. In some cases, input offset specifications apply over input voltage range. —(Regulators) Range of DC input voltages over which regulator will operate within specifications.

Large-Signal Voltage Gain—(Op Amps) Ratio of maximum output voltage swing to change in input voltage required to drive output to this voltage.

Line Regulator—(Regulators) Percentage change in output voltage for a specified change in input voltage.

Load Regulator—(Regulators) Percentage change in output voltage load a specified change in load current;

Long Term Stability—(Regulators) Output voltage stability under accelerated life-test conditions at 125°C with maximum rated voltages and power dissipation for 1000 hours.

Maximum Power Dissipation—(Regulators) Maximum total device dissipation for which regulator will operate within specifications.

Negative Output Level—(Comparators) Negative DC output voltage with comparator saturated by differential input equal to or greater than specified voltage.

Offset Voltage—(Comparators) Difference between absolute values of threshold voltage in positive- and negative-going directions.

Output Impedance—(Op Amps) Ratio of output voltage to output current under stated conditions for source resistance (R_S) and load resistance (R_L).

Output Leakage Current—(Comparators) Current into output terminal with output voltage within given range and input drive equal to or greater than given value.

Output Noise Voltage—(Regulators) RMS output noise voltage with constant load and no input ripple.

Output Resistance—(Comparators) Resistance seen looking into output terminal with DC output level at logic threshold voltage. —(Op Amps) Resistance seen looking into output terminal with output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate influence of drift and thermal feedback.

Output Short-Circuit Current—(Op Amps) Maximum output current available from amplifier with output shorted to ground or to either supply.

Output Sink Current—(Comparators) Maximum negative current that can be delivered by comparator.

Output Voltage Range—(Regulators) Range of output voltage over which regulator will operate.

Output Voltage Scale Factor—(Regulators) Output voltage obtained for unit value of resistance between adjustment terminal and ground.

Output Voltage Swing—(Op Amps) Peak output swing, referred to zero, that can be obtained.

Peak Output Current—(Comparators) Maximum current that may flow into output load without causing damage to comparator.

Positive Output Level—(Comparators) High output voltage level with given load and input drive equal to or greater than specified value.

Power Consumption—(Comparators) Power required to operate comparator with no output load. Power will vary with signal level, but is specified as maximum for entire range of input signal conditions. —(Op Amps) DC power required to operate amplifier with output at zero and with no load current.

Power Supply Rejection Ratio—(Op Amps) Ratio of change in input offset voltage to change in supply voltages producing it.

Propagation Delay—(Comparators) Interval between application of an input voltage step and its arrival at either output, measured at 50% of final value.

Quiescent Current—(Regulators) Part of input current to regulator that is not delivered to load.

Reference Voltage—(Regulators) Output of reference amplifier measured with respect to negative supply.

Response Time—(Comparators) Interval between application of input step function and time when output crosses logic threshold voltage. Input step drives comparator from some initial, saturated input voltage to input level just barely in excess of that required to bring output from saturation to logic threshold voltage overdrive.

Ripple Rejection—(Regulators) Ratio of peak-to-peak input ripple voltage to peak-to-peak output ripple voltage.

Rise Time—(Op Amps) Time required for an output voltage step to change from 10% to 90% of its final value.

Sense Voltage—(Regulators) Voltage between current sense and current limit terminals necessary to cause current limiting.

Settling Time—(Op Amps) Time between initiation of input step function and time when output voltage has settled to within

Short-Circuit Current Limit—(Regulators) Output current of regulator with output shorted to negative supply.

Slew Rate—(Op Amps) Maximum rate of change of output voltage under large signal condition.

Standby Current Drain—(Regulators) Supply current drawn by regulator with no output load and no reference voltage load.

Strobe Current—(Comparators) Maximum current drawn by strobe terminals when it is at zero logic level.

Strobe Delay—(Comparators) Time delay measured from strobe to output threshold with signal present exceeding input threshold.

Strobe OFF Voltage—(Comparators) Minimum voltage on strobe terminal that will guarantee that it does not interfere with operation of comparator.

Strobe ON Voltage—(Comparators) Maximum voltage on either strobe terminal required to force output to specified high state independent of input voltage.

Strobe Release Time—(Comparators) Time required for output to rise to logic threshold voltage after strobe terminal has been driven from zero to one logic level. Appropriate input conditions are assumed.

Strobed Output Level—(Comparators) DC output voltage, independent of input conditions, with voltage on strobe terminal equal to or less than specified low state.

Supply Current—(Comparators) Current required from positive or negative supply to operate comparator with no output load. Power will vary with input voltage, but is specified as maximum for entire range of input voltage conditions. —(Op Amps) Current required from power supply to operate amplifier with no load and output at zero.

Switching Speed—(Comparators) Time required to turn on least significant bit.

Temperature Stability—(Regulators) Percentage change in output voltage for thermal variation from room temperature to either temperature extreme.

Temperature Stability of Voltage Gain—(Op Amps) Maximum variation of voltage gain over specified temperature range.

Transient Response—(Op Amps) Closed-loop step-function response of amplifier under small-signal conditions.

Unity Gain Bandwidth—(Op Amps) Frequency range from DC to frequency where amplifier open-loop gain rolls off to one.

Voltage Gain—(Comparators) Ratio of change in output voltage to change in voltage between input terminals producing it. —(Op Amps) Ratio of output voltage to input voltage under stated conditions for source resistance (R_S) and load resistance (R_L).

Package Information

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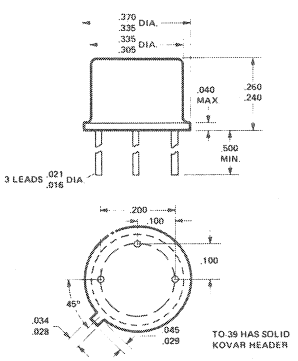
3 LEAD METAL CAN



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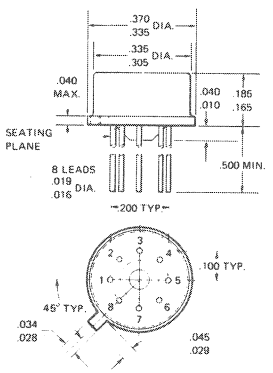

NOTE: Case Electrically Isolated From Leads

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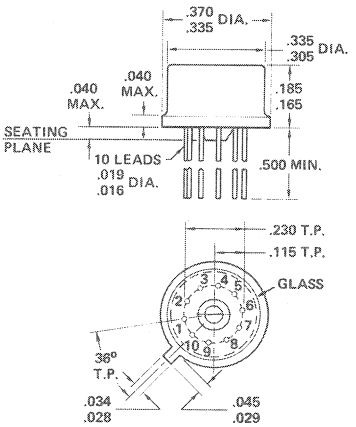

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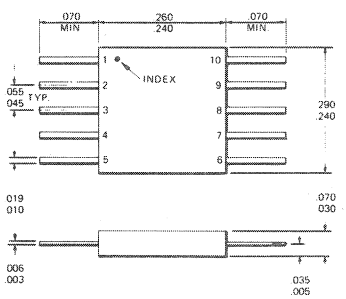

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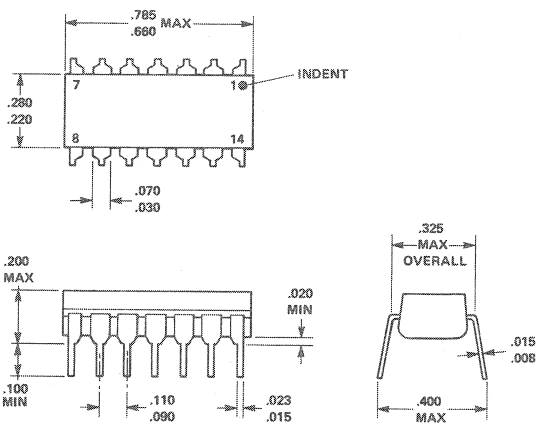

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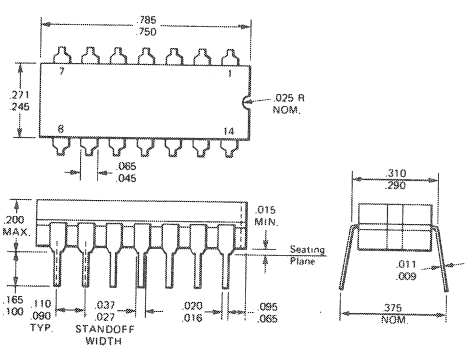

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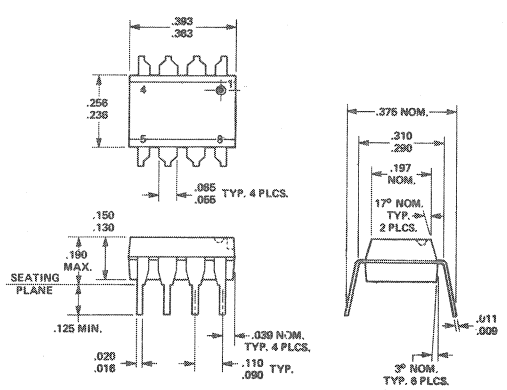

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TELEDYNE SEMICONDUCTOR

1300 Terra Bella Avenue, Mountain View, Ca. 94043 • Tel. (408) 968-9241 • TWX: 910-379-6494 • Telex: 34-8416
Burgstrasse 6-8, 62 Wiesbaden, West Germany • Tel. (06121) 39171 • Telex: 4186846
10 Sam Chuk Street, San Po Kong, Hong Kong • Tel. K-207764 • Telex: Hx3549
Additional offices in England, France, West Germany, Japan and the United States. Representatives and distributors worldwide.

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